NIST Special Publication 823-2

Computer Systems Technology

U.S. DEPARTMENT OF COMMERCE
Technology Administration
National Institute of Standards and Technology

NIST

Integrated Services Digital Network Conformance Testing

Layer 1—Physical Layer

Part 2—Basic Rate U Interface, User Side

NIST Special Publication 823-2

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Layer 1—Physical Layer

Part 2—Basic Rate U Interface, User Side

Based on work performed by the
North American ISDN Users' Forum

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March 1992

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National Institute of Standards and Technology Special Publication 823-2
Natl. Inst. Stand. Technol. Spec. Publ. 823-2, 96 pages (Mar. 1992)
CODEN: NSPUE2

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1992

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402

ISDN Conformance Testing

Layer 1 — Physical Layer

Part 2: Basic Rate U Interface

ABSTRACT

The American National Standard for Telecommunications (ANS) T1.601-1988 specifies the minimal set of requirements to provide for satisfactory transmission between the network and the Network Termination (NT). It describes both the physical interface and the electrical characteristics of the signals appearing at the network side of the NT, commonly called the U interface point, or U reference point. Equipment designed to operate on the North American Integrated Services Digital Network (ISDN) Basic Access U Interface must conform with this set of minimal requirements.

This document describes a set of conformance test specifications for all NTs connected to the Basic Rate ISDN user-network interface. These tests were developed and approved by members of the North American ISDN Users' Forum.

KEYWORDS

Abstract Test Suites, Basic Rate Interface, BRI, Conformance Testing, Digital Subscriber Line, ISDN, Network Termination, NT, Physical Layer, Static Conformance Requirements, U Interface, U Reference Point

PREFACE

This document is one of a group of NIST Special Publications that will be issued on Integrated Services Digital Network (ISDN) Conformance Testing. Each publication in this group will focus on a different set of conformance test specifications. The following is a list of the publications in this group:

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Introduction - This document will discuss the basic concepts of conformance testing and the development of abstract test specifications for conformance testing of ISDN protocols.

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Layer 1 — Physical Layer

  - Part 1 Basic Rate S/T Interface, User Side describes a set of test specifications which verify conformance of TEs and NTs to the ISDN Physical Layer Basic Access at the S/T reference point, as defined in ANS T1.605-1989, and NIU 90-105.

  - Part 2 Basic Rate U Interface, User Side will describe a set of test specifications which verify equipment implementation conformance to the ISDN Physical Layer Basic Access at the U interface, as defined in ANS T1.601-1988 and NIU 90-101.

  - Part 3 Primary Rate Interface, User Side will describe a set of test specifications which verify equipment implementation conformance to the ISDN Physical Layer Primary Access at the S, T, and U interface, as defined in ANS T1.408-1990 and the corresponding NIUF Implementation Agreement.

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Layer 2 — Data Link Layer, Link Access Procedure on the D Channel (LAPD)

  - Part 1 Basic Rate Interface, User Side will define the abstract test specifications to verify equipment implementation conformance to the Layer 2 of an ISDN at the user-network interface, for the BRI access arrangements, as defined in ANS T1.602-1989 and NIU 90-210.

  - Part 2 Primary Rate Interface, User Side will define the abstract test specifications to verify equipment implementation conformance to the Layer 2 of an ISDN at the user-network interface, for the PRI access arrangements, as defined in ANS T1.602-1989 and the corresponding NIUF Implementation Agreement.

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Layer 3 — Network Access Layer

  - Part 1 Basic Rate Interface Circuit Switch Call Control, User Side will define the abstract test specifications to verify equipment implementation conformance to the Layer 3 of an ISDN BRI at the user-network interface for the Basic Call Control Procedures, as defined by ANS T1.607-1990, NIU 90-301, and other corresponding NIUF Implementation Agreements.

  - Part 2 Primary Rate Interface Circuit Switch Call Control, User Side will define the abstract test specifications to verify equipment implementation conformance to the Layer 3 of an ISDN PRI at the user-network interface for the Basic Call Control Procedures, as defined by ANS T1.607-1990, NIU 90-302, and other corresponding NIUF Implementation Agreements.

- Part 3 Packet Switched Call Control will define the abstract test specifications to verify equipment implementation conformance to the Layer 3 of an ISDN at the user-network interface for the Packet Switched Call Control Procedures, as defined by ANS T1.608-1990, NIU 90-320, and other corresponding NIUF Implementation Agreements.

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Supplementary Services - This document will define the abstract test specifications to verify implementation conformance to the Supplementary Services at the user-network interface, as defined in ANS T1.610-1990, NIU 90-311, and other appropriate ANS documents and their corresponding NIUF Implementation Agreements.

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Packet Mode Bearer Services Control Procedures - This publication will define the abstract test specifications to verify implementation conformance to the Packet Mode Bearer Services Control Procedures.

- Integrated Services Digital Network (ISDN) Conformance Testing —
  Terminal Adaption - This document will define the abstract test specifications to verify equipment implementation conformance to the ISDN Circuit-Mode Data Terminal Adaption using Statistical Multiplexing, as defined by ANS T1.612-1990 and the corresponding NIUF Implementation Agreement.

NOTICE OF DISCLAIMER

THIS DOCUMENT CONTAINS NIUF CONFORMANCE TESTS AS AGREED AMONG PARTICIPATING EXPERT TECHNICAL PERSONNEL ACCORDING TO THE TEXTS OF ISDN STANDARDS, CONFIGURATIONS AND DESCRIPTIONS THAT ARE INTENDED TO PROMOTE INTEROPERABILITY AND EFFICIENCY. THESE CONFORMANCE TESTS WERE DEVELOPED AND APPROVED BY ORGANIZATIONS PARTICIPATING IN THE NORTH AMERICAN ISDN USERS' FORUM (NIUF) MEETINGS. NEITHER THE NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY (NIST) NOR ANY OF THE PARTICIPANTS IN THE NIUF MAKE ANY REPRESENTATION OR WARRANTY, EXPRESS OR IMPLIED WITH RESPECT TO THE SUFFICIENCY, ACCURACY, OR USE OF ANY INFORMATION OR OPINION CONTAINED HEREIN. THE USE OF THIS INFORMATION OR OPINION IS AT THE RISK OF THE USER. UNDER NO CIRCUMSTANCES SHALL NIST, OR ANY PARTICIPANT IN THE NIUF BE LIABLE FOR ANY DAMAGE OR INJURY INCURRED BY ANY PERSON ARISING OUT OF THE SUFFICIENCY, ACCURACY, OR USE OF ANY INFORMATION OR OPINION CONTAINED HEREIN.

ACKNOWLEDGMENTS

NIST would like to acknowledge the NIUF ISDN Conformance Testing (ICOT) Working Group, and especially the following individuals for their valuable contributions to this document:

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1 GENERAL

1.1 Introduction

The American National Standard for Telecommunications (ANS) T1.601-1988 specifies the minimal set of requirements to provide for satisfactory transmission between the network and the Network Termination (NT). It describes both the physical interface and the electrical characteristics of the signals appearing at the network side of the NT, commonly called the U Interface point. Equipment designed to operate on the North American Integrated Services Digital Network (ISDN) Basic Access U Interface must conform with this set of minimal requirements.

This document describes a set of conformance test specifications for the ISDN Physical Layer at the U reference point. The test suites described herein are intended for use by all members of the North American ISDN Users' Forum (NIUF). The suites are based on the ANS T1.601-1988 standard and adhere to it to the greatest extent possible. This document will be updated subsequent to any published revisions of ANS T1.601-1988.

Communication between adjacent layers is conceptual (primitive procedures) and allows description of interactions between functions dedicated to different layers. These primitive procedures do not constrain an implementation, are system internal, and therefore cannot be tested in isolation. However, as seen from the outside, the design of equipment shall be such that the sequence of events across the user-network interface must be the same as if the primitives were implemented as described in the relevant standard.

1.2 Purpose

The purpose of this document is to describe a set of accepted test suites which test conformance of NTs to the Layer 1 requirements specified in ANS T1.601-1988. The specific ANS T1.601-1988 requirements for NT equipment claiming to support the basic rate U interface are outlined in section 2. The Static Conformance Requirements (SCR) column in the tables of section 2 indicates whether the requirements are mandatory or optional. An NT is considered conformant to ANS T1.601-1988 if it passes all tests for Static Conformance Requirements labeled "mandatory" as well as all tests labeled "optional" for the options it implements.

If a device fails any test for SCRs labeled "mandatory" or SCRs labeled "optional" for options it implements, it will be considered as nonconforming to ANS T1.601-1988.

Certain optional requirements may not require the entire option to be implemented. For these requirements, the equipment manufacturer must specify what portion of the requirement is implemented within their equipment and only that portion of the test suite required to test that functionality will be executed. Test suites falling within this category will be annotated.

1.3 Configurations at User Premises

This document applies to conformance testing of equipment which terminates the digital subscriber line (DSL) on the user side of the U interface point. The NT function may be in an NT1, and NT2, or Terminal Equipment (TE).

1.4 Relationship to other NIUF Conformance Testing Documents

The Layer 1 conformance tests in this document apply to all NTs connected to the Basic Rate ISDN user-network interface. Additionally, the requirements for conformance testing of Layer 1 at the S/T interface and the testing of Layer 2 and Layer 3 are described in separate NIUF documents[1] as follows:

- NIU 90-002 (ICOT/ACT1/90-40), Layer 1 Conformance Testing — S/T Interface;
- NIU 91-0007 (ICOT/ACT23/91-22.2 V1.2) Layer 2, BRI LAPD User Side Conformance Test Suite;
- NIU 91-0009 (ICOT/ACT23/91-10.3 R4) Layer 3 Basic Call Control Procedures, BRI/Class I, User Side, Conformance Test Suite.

1.5 Testing and Approval Methodology

Conformance shall be tested using the tests specified in section 2 of this document. Those functions and procedures that are indicated in this document as being optional shall be subject to a conformance test only if they are implemented in the System Under Test (SUT). The means of determining whether an optional function or procedure has been implemented is either by the supplier's declaration or as the result of performing conformance tests on the SUT. Where no declaration is made by the supplier as to the implementation of an optional function or procedure, and the conformance test reveals that the option is incorrectly (or partially) implemented, the option shall be deemed to have been implemented and the equipment shall be tested accordingly.

The user-network interface at the U reference point provides the only test access for the purpose of performing conformance tests. However, actions at the user side of the SUT (e.g., at the S/T reference points, at the man-machine interface, execution of higher layer processes) shall be used to invoke actions at Layer 1 of the B and D Channels within the SUT.

When carrying out a test, it may be necessary for the SUT to be maintained in the active state of a call. In such cases it may be necessary for the tester to achieve this by procedural means related to functional entities outside the scope of this document.

Throughout the test suites in this document, reference is made to a "Layer 1 tester." This term is used to denote a device (or set of components) that is able to transmit and receive 2B1Q signals and to emulate other basic Line Terminator (LT) functionalities. A description of the functional requirements of the tester is given in appendix A, though it should be noted that a test which specifies a Layer 1 tester may require only a subset of the functions listed.

1.6 Information to be Provided by the Supplier

The supplier shall provide two kinds of information:

- information with respect to the protocol: Protocol Implementation Conformance Statement (PICS).

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[1] For copies of the NIU-Forum documents, please contact Dawn Hoffman, NIU-Forum Administrator, NIST, Building 223, Room B364, Gaithersburg, MD 20899

- information with respect to the man-machine interface: Protocol Implementation eXtra Information for Testing (PIXIT).

The complete list of the information to be provided by the supplier is a matter between the supplier and the testing house.

1.7 Test Support Required of the Supplier

If the equipment to be tested does not provide either:

- access to the B1, B2, and D channels externally (see Note);

or

- implementation of loopback (B1, B2, or 2B+D),

then the equipment will not support Layer 1 tests requiring specific bit patterns in the B channels.

In this case the supplier shall additionally provide a modified unit for test using the same chip set and interface components as in the equipment under consideration. This test equipment shall provide a means for access to the B1 and B2 channels (see Note) to allow insertion/extraction of specific test patterns so that necessary Layer 1 tests can be carried out or else an implementation of loopbacks.

Note: The interface providing access to the B-Channels may be any mutually agreed upon interface. Such an interface shall be provided either directly on the terminal equipment or else by an adaptor provided by the equipment supplier. One such interface is expanded below as a guide.

- Three ports shall be provided, one for B1, one for B2, and one for D access.

- The ports will use an interface with EIA-422 balanced drivers/receivers and include the EIA-232 signal lines TD, RD, TC, RC, and SG. The clocks TC and RC can be independent but must be synchronous with the data on TD and RD respectively and operate at a frequency of 64 kbit/s for the B-Channels and 16 kbit/s for the D-Channel.

- Each port will have a standard 25-pin D-type female connector.

1.8 Test Environment

All tests specified in this document shall be performed at:

- an ambient temperature in the range 15 °C to 35 °C (60 °F to 95 °F),

- a relative humidity in the range 25% to 75%,

- an air pressure in the range 86.2 kPa to 105.5 kPa (12.5 lb/in^2 to 15.3 lb/in^2).

For an SUT which is directly powered (either wholly or partly) from the AC power line, all tests shall be carried out within ±5% of the normal operating voltage. If the SUT is powered by other means and those means are not supplied as part of the apparatus (e.g., batteries, stabilized AC supplies, DC) all tests shall be carried out within the power supply limit declared by the supplier. If the power supply is AC, the tests shall be conducted within 4% of the normal operating frequency

1.9 Test Equipment Substitutions

The conformance tests specified in this document are intended to test equipment which exists on the ISDN Basic Access interface at the U reference point in accordance with requirements given in ANS T1.601-1988. In the case that tests engineered herein are not aligned with the specifications in ANS T1.601-1988 (there are instances where simpler but slightly more restrictive tests are employed), the specifications in ANS T1.601-1988 will take precedence over those in this document.

The conformance tests described herein have been designed to afford the required accuracy while using the least specialized and most widely available test equipment. In some cases this results in cumbersome, manually intensive tests that can be better performed with more costly specialized equipment. The testing organization is free to take advantage of such specialized equipment in any of the following tests. The testing organization that uses different test equipment or test methodologies must, however, demonstrate to their clientele that their tests are at least as comprehensive and as accurate as those contained in this document.

1.10 Referenced Standards and NIUF Implementation Agreements

This document is intended to be used in conjunction with the following standards and implementation agreements:

ANS T1.601-1988[2], *Telecommunications — Integrated Services Digital Network (ISDN) — Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT-Layer 1 Specification*

NIST Special Publication 500-195[3], *North American ISDN Users' Forum Agreements on ISDN*, section 4.1.1.1 (NIU 89-101).

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[2] Available from the American National Standards Institute, 11 West 42nd Street, New York, NY 10036

[3] For copies of the NIU-Forum documents, please contact Dawn Hoffman, NIU-Forum Administrator, NIST, Building 223, Room B364 Gaithersburg, MD 20899.

2 MAPPING TO ANS T1.601-1988

2.1 Overview

The purpose of the following specification breakdown is to identify functional and electrical conformance parameters for evolving specific test procedures. The following documents[4] are used as reference:

- ANS T1.601-1988[5], "*ISDN Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)*," September 16, 1988.

- ANS T1.601-1991[5], "*ISDN Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)*," September 16, 1988.

- NIU/ACT1/89-034, "Specification Breakdown of ANSI T1.601," Al Koenig, NIST.

- NIU/ACT1/90-002R1, "Contribution on T1.601 Testing," Tim Gee, IBM.

- NIU/ACT1/90-007R2, "Contribution on Start Up Procedures," Steve Olsen, Bell Atlantic.

- NIU/ACT1/90-018, "Contribution on Return Loss Measurement," Steve Olsen, Bell Atlantic.

- NIU/ACT1/90-019R1, "Contribution on Performance Test Requirements," Jerry Tall/Mehdi Mohebbi, Telcommunications Techniques Corp.

- NIU/ACT1/90-023, "Contribution on DC Characteristics," Mike Ruggiero, AT&T.

- NIU/ACT1/90-027R1, "Layer 1 Tester Functions and Test Configurations," Hang Nguyen, Bellcore.

- NIU/ACT1/90-029, "Pulse Shape and Nonlinearity Compliance Tests," Hang Nguyen, Bellcore.

- NIU/ACT1/90-030, "Longitudinal Balance," Hang Nguyen, Bellcore.

- NIU/ACT1/90-032, "M-Channel Tests," Mike Ruggeiro, AT&T.

- NIU/ACT1/90-034, "Baud Rate, Timing, and Synchronization," Hang Nguyen, Bellcore.

- NIU/ACT1/90-035, "User Data (2B+D)," Hang Nguyen, Bellcore.

- NIU/ACT1/90-036, "Conformance Testing the ISDN Basic Access DSL Embedded Operations Channel," Frank Holleman, Bellcore.

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[4] For copies of the NIU-Forum documents, please contact Dawn Hoffman, NIU-Forum Administrator, NIST, Building 223, Room B364 Gaithersburg, MD 20899.

[5] Available from the American National Standards Institute, 11 West 42nd Street, New York, NY 10036.

- NIU/ACT1/90-043, "NT Output Jitter Limitation," Alex Dietz, Bellcore.

- NIU/ACT1/91-005, "Suggested Changes in Power Spectral Density, Return Loss, Start-Up Procedures, and Appendix A," Hang Nguyen, Bellcore.

- NIU/ACT1/91-011, "Suggested Changes in Start-Up Conformance Test Procedures," Hang Nguyen, Bellcore.

Note 1: The Static Conformance Requirements (SCR) column indicates whether the section is mandatory (M), optional (O), or conditional (C).

Note 2: The Suite column points to the conformance test suites in this document.

Note 3: Some test suites may require special access to the system under test (SUT). These cases will be flagged by "SA" in the Comments column.

2.2 Specification Breakdown

Table 2.2.1. Physical Characteristics

T1.601	PARAMETER	SCR	SUITE	COMMENTS
4.1	Wiring Polarity	M	5.4	

Table 2.2.2. Transmission Method

T1.601	PARAMETER	SCR	SUITE	COMMENTS
5.2	Line Code	M	3.1	4-level, 2B1Q.
5.3.1	Pulse Shape	M	3.2	See Fig.6 in ANS T1.601. SA*
5.3.2.1	Power Spectral Density	M	3.3.1	See Fig.7 in ANS T1.601. SA*
5.3.2.2	Total Power	M	3.3.2	SA*
5.3.3	Transmitter Linearity	M	3.4	See App.D in ANS T1.601. SA*

* Special Access: Ability to put the SUT in a free run mode.

Table 2.2.3. Received Line Signal Characteristics

T1.601	PARAMETER	SCR	SUITE	COMMENTS
5.4.2	Performance Test Requirements	M	3.5	Procedures given in Section 5.4.3 and 5.4.4 of ANS T1.601.

Table 2.2.4. Functional Characteristics

T1.601	PARAMETER	SCR	SUITE	COMMENTS
6.1	Baud Rate, Timing and Synchronization	M	5.1	Test for 80 kbaud, ±32 ppm, is optional.
	FRAME STRUCTURE			
6.2.1	Synchronization Word	M	5.2.2.1	
6.2.2	User Data (2B+D)	M	5.5	
6.2.4	M-Channel	M	6	Table 2.2.7 covers M-Channel
6.2.4	Frame Offset	M	5.3	
6.2.5	Superframes	M	5.5	
6.3	Scrambling	M	5.6	

Table 2.2.5. Start-Up Procedures

T1.601	PARAMETER	SCR	SUITE	COMMENTS
	TIMERS			
6.4.3	Failure to Complete Start-Up	M	5.2.3.1	
6.4.3	Loss of Received Signal	M	5.2.3.2	
6.4.3	Loss of Synchronization	M	5.2.3.3	
6.4.3	Loss of Signal after TN ceases	M	5.2.3.4	
	SIGNALS DURING START-UP			
6.4.4	Verify TN/SN1 and Sync Word	M	5.2.2.1	
6.4.4	Verify Signal SN2	M	5.2.2.2	
6.4.4	Verify Signal SN3	M	5.2.2.3	
	START-UP SEQUENCE			
6.4.6.2	Activation from Customer Equip.	M	5.2.1.1	
6.4.6.3	Activation from the Network	M	5.2.1.2	
6.4.6.5	Deactivation	O	5.2.1.3	
	START-UP TIME REQUIREMENT			
6.4.7	Cold Start	M	5.2.1.1 & .2	
6.4.7	Verify Warm Start	O	5.2.4	

Table 2.2.6. Electrical Characteristics

T1.601	PARAMETER	SCR	SUITE	COMMENTS
7.1	Impedance, Return Loss	M	4.1	SA: Ability to put SUT in quiet mode.
7.2	Longitudinal Output Voltage	M	4.2	See Fig.18 in ANS T1.601.
7.3	Longitudinal Balance	M	6.3	See Fig.19 in ANS T1.601.
7.4.1	Jitter Tolerance, NT Input Signal	M	3.5	
7.4.2	Jitter Limitations, NT Output	M	4.4	
	DC CHARACTERISTICS			
7.5.1	Sealing Current	M	4.5.3	
7.5.2	Metallic Termination	M	4.5.1 and 4.5.2	

Table 2.2.7. M-Channel Bit Functions

T1.601	PARAMETER	SCR	SUITE	COMMENTS
8.1.1	Cyclic Redundancy Check	M	6.1	
	OVERHEAD BIT FUNCTIONS			
8.2.1	Far End Block Error Bit	M	6.2	
8.2.2	Activation Bit	M	6.3	
8.2.3	Deactivation Bit	M	5.2.1.3	
8.2.4	NT Power Status Bits	M	6.4	
8.2.5	NT Test Mode Indicator	M	6.5	
8.2.6	Cold Start Only Bit	M	5.2.4	
8.2.7	Reserved Bits	M	6.6	
8.3	Embedded Operations Channel (eoc) Functions	M	6.7.1	Test Script #1
		M	6.7.2	Test Script #2
		M	6.7.3	Test Script #3

3 TRANSMISSION METHOD

3.1 Line Code

ANS T1.601-1988, section 5.2, Line Code, is an explanation of the 2B1Q line code and how a "U" frame is put together and transmitted on the line. Line code is not tested in this test suite. However, if the SUT passes the test suites described in section 5.2.2 of this document, it is considered compliant with ANS T1.601-1988, section 5.2.

3.2 Pulse Shape

PURPOSE:
To verify that the SUT's transmitted pulses meet the pulse template specified in ANS T1.601-1988, figure 6.

EQUIPMENT:
- 12-bit waveform digitizer with a balanced input
- digital computer

CONFIGURATION:

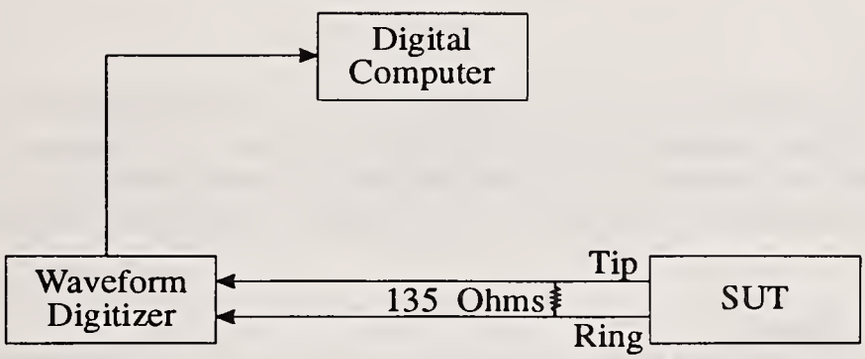


Figure 1. Test Configuration for Pulse Shape Compliance.

Note: The digitizer's sampling frequency should be locked to the SUT's free-running baud rate.

PROCEDURE:
Connect the equipment as shown in figure 1. The SUT's output signal is captured while transmitting pseudo-random data into a 135 ohm load in the absence of received signal. A minimum of 1000 2B1Q symbols should be stored to process the pulse shape. The waveform digitizer should sample the SUT's output signal at a minimum sampling rate of 8 samples/baud. The SUT's pulse shape can be verified by application of adaptive signal processing to the digitized samples. An example of a software routine that estimates the SUT's pulse shape is given in appendix B.

Note: It is desirable that the SUT is capable of transmitting a pseudo-random signal in the absence of the received signal. This will simplify the pulse shape estimation software because echo cancellation is not required.

PASS-FAIL CRITERIA:
The SUT's output pulse shape must be inside the pulse template specified in ANS T1.601-1988, figure 6.

3.3 Signal Power

3.3.1 Transmitted Spectrum

PURPOSE:
To verify that the signal transmitted by the SUT meets the power spectral density requirements of ANS T1.601-1988, section 5.3.2.1.

EQUIPMENT:
- Spectrum analyzer with balanced input

CONFIGURATION:

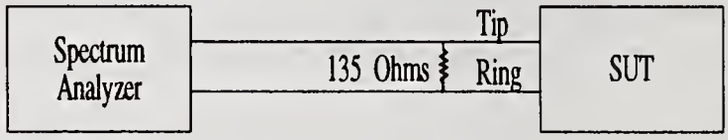


Figure 2. Test Configuration for Transmitted Spectrum.

PROCEDURE:
Connect the equipment as shown in the configuration. The SUT shall be placed in a test mode that enables it to transmit continuously into a 135 ohm termination in the absence of the received signal. Measure the spectrum in accordance with the operational instructions of the spectrum analyzer. Measurements are to be made with a resolution bandwidth and video bandwidth of 1 kHz.

PASS-FAIL CRITERIA:
The spectrum measured shall be no greater than the upper bound as outlined in ANS T1.601-1988, figure 7.

3.3.2 Average Transmitted Power

PURPOSE:
To verify that the average power of the signal transmitted by the SUT meets the requirements stated in ANS T1.601-1988, section 5.3.2.2.

EQUIPMENT:
- 80 kHz filter, balanced
- a True RMS Voltmeter

CONFIGURATION:

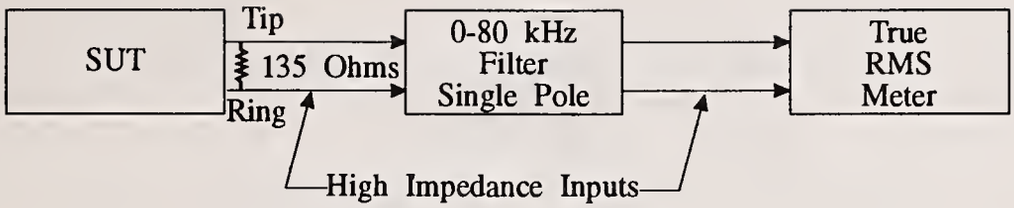


Figure 3. Configuration for Measuring Transmitted Power.

PROCEDURE:
Connect the equipment as shown, with a 135 ohm load at the transmitter of the SUT. The SUT shall be placed in a test mode that enables it to transmit continuously into a 135 ohm termination in the absence of a received signal. The RMS meter should have a bandwidth of at least 1 MHZ.

PASS-FAIL CRITERIA:
The power as calculated by:

$$Power = 20\log\left(\frac{MeasuredVoltage}{V2}\right)$$

where

$$V2 = \sqrt{.001 * 135}$$

shall be between 13.0 and 14.0 dBm.

3.4 Transmitter Linearity

PURPOSE:
To verify that the SUT's output signal has a residual (nonlinearity) of at least 36 dB below a perfectly linear signal.

EQUIPMENT:
- 12-bit waveform digitizer with balanced inputs
- digital computer

CONFIGURATION:

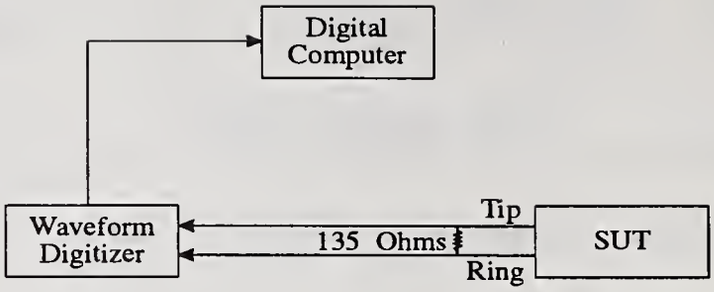


Figure 4. Test Configuration for Transmitter Linearity.

Note: The digitizer's sampling frequency should be locked to the SUT's free-running baud rate.

PROCEDURE:
Connect the equipment as shown in figure 4. The SUT's output signal is captured while transmitting pseudo-random data into a 135 ohm load in the absence of a received signal. The waveform digitizer should sample the SUT's output signal at a minimum sampling rate of 8 samples/baud. The SUT's nonlinearity can be computed by application of adaptive signal processing to the digitized samples. An example of a software routine that computes the transmitter nonlinearity is given in appendix B.

Note: It is desirable that the SUT is capable of transmitting a pseudo-random signal in the absence of the received signal. This will simplify the transmitter linearity estimation software since echo cancellation is not required.

PASS-FAIL CRITERIA:
The SUT's nonlinearity must be at least 36 dB below a perfectly linear signal.

3.5 Performance Test Requirements

PURPOSE:
To verify that the SUT Transceiver will operate with an acceptable error rate (BER<10^{-7}) in the presence of noise and impairments and through various loops specified in ANS T1.601-1988.

EQUIPMENT:
- Layer 1 tester B (point "F") equipped with U interface and a pseudo-random pattern generator.
- Layer 1 tester A (point "A") equipped with S/T interface, or an interface compatible with the test access provided by the SUT (see Note 3), and BER testing abilities.
- Noise and impairment generator

CONFIGURATION:

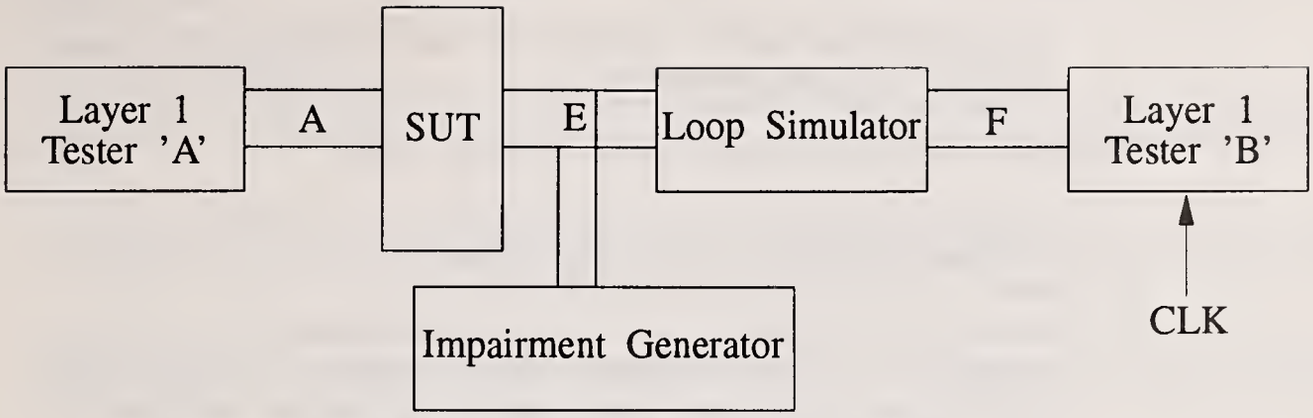


Figure 5. Configuration for Performance Tests.

PROCEDURE:
Connect the SUT, a loop simulator, and two Layer 1 testers according to figure 5.

Both Layer 1 testers should be transmitting pseudo-random patterns and the Layer 1 tester A at point "A" shall measure BER. The BER computed by the Layer 1 tester A at point "A" verifies the performance of the SUT's receiver. The Layer 1 tester B connected at point "F" must either generate the clock (CLK) or use an independent clock source (this set is simulating an LT). The SUT will recover its clock from the U interface signal. The Layer 1 tester A connected at point "A" will get its timing from the SUT. Tests must be repeated using the 15 various loop configurations as shown in ANS T1.601-1988, figure 8, and a Null Loop Configuration.

Note 1: To test all 16 loop configurations, it is acceptable to use loop simulators or actually build these loop configurations. In addition, to compensate for discrepancie between measured and actual loop loss, refer to appendix D of this document, "Compensation Methods for Loop Insertion Loss Discrepancies.

Note 2: Layer 1 tester B at point "F" must be calibrated to insure it meets all of the ANS T1.601-1988 transmission requirements.

Note 3: This test applies to stand alone NTs as well as NT units that are built into a TE. If NT's capabilities are built into a TE, a test access must be provided to allow transmission and reception of pseudo-random data at point "A."

The following impairments must be injected to test the receiver's tolerance in the presence of noise and impairments. Refer to ANS T1.601-1988, section 5.4.4 for information on applying these impairments.

A. Near End Crosstalk (NEXT) (ANS T1.601-1988, sec. 5.4.4.1)

The noise generator must produce the NEXT impairment detailed in ANS T1.601-1988, section 5.4.4.1.

The noise generator shall generate the NEXT noise with 6 dB of margin (i.e., NEXT noise is 6 dB greater) on test loops 4-15, and on the null test loop. The noise generator should generate the NEXT noise with 0 dB margin on test loops 1 - 3.

B. Longitudinal Noise (ANS T1.601-1988, sec. 5.4.4.2)

The noise generator must be capable of providing longitudinal noise as defined in ANS T1.601-1988, section 5.4.4.2

C. Power related metallic noise (ANS T1.601-1988, sec. 5.4.4.3)

The noise generator must be capable of providing power-related metallic noise as defined in ANS T1.601-1988, section 5.4.4.3.

Note 4: The specification calls for testing all combinations of any two tones, with any of the 16 loop configurations. To save testing time, it is acceptable to apply all frequencies at once. Only if the SUT did not pass the test with all frequencies should it be tested with all combinations of any two frequencies.

D. Jitter (ANS T1.601-1988, sec. 7.4.1)

The Layer 1 tester B at point "F" should be able to transmit a pseudo-random pattern with jitter superimposed. The superimposed jitter should sweep the frequency range of 0.1 Hz to 20 kHz with jitter amplitude as specified in ANS T1.601-1988, figure 20.

For each test loop, the entire range of 0.1 Hz to 20 kHz must be swept at least once. A minimum of one complete cycle of each applied sinusoidal jitter frequency chosen should be applied.

E. Wander (ANS T1.601-1988, sec. 7.4.1)

The Layer 1 tester B at point "F" needs to add a wander impairment of 1.44 Unit Intervals (UI) peak-to-peak per day. The wander impairment should be added while testing each loop configuration.

To save time the tester may try to test 1.44/24 = 0.06 UI of wander on each loop configuration. To test for maximum wander, the tester will try 1.44 UI peak-to-peak per day, only on loop configuration #4 (ANS T1.601-1988, fig. 8).

F. Timing Tolerance (ANS T1.601-1988, sec. 7.4.1)

The Layer 1 tester B at point "F" shall be adjusted to produce the maximum allowable frequency of 80 kbaud ±5 ppm or 80 kbaud ±32 ppm if the SUT is designed for other applications.

With the setup described above, and with all impairments and jitter added, perform a BER test on each loop and repeat the test in the reverse direction for each loop. This gives a total of 16x2=32 tests to perform. The length of the BER test varies depending on the BER data rate as shown below:

BER Test Times

Channels Tested	Minimum Test Length
1B (64 kb/s)	25 min
2B (128 kb/s)	13 min
2B+D (144 kb/s)	10 min

Note that if tests are performed on less than 144 kb/s, then all untested channels must transmit a pseudo-random pattern.

PASS-FAIL CRITERIA:
Conformance testing is PASSED if the SUT demonstrates a BER of less than 10^{-7} on loops 4 through 15 and the null loop while all noise (including 6 dB NEXT), jitter and wander impairments are added to the line.

It is desirable to obtain satisfactory performance with a margin of at least 0 dB with test loops 1 through 3. Inability to meet this objective, however, does not constitute failure of conformance.

Note 5: Since loop 15, loop 7, and the null loop are symmetrical it is adequate to test only in one direction on these loops.

4 ELECTRICAL CHARACTERISTICS

4.1 Impedance and Return Loss

PURPOSE:
To verify that the driving point impedance meets the specifications as outlined in ANS T1.601-1988, section 7.1.

EQUIPMENT:
- Impedance analyzer with balanced input
- Sealing Current Source (SCS)

CONFIGURATION:

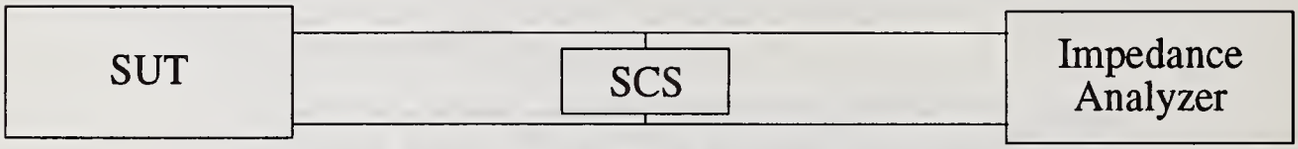


Figure 6. Driving Point Impedance Test.

PROCEDURE:
Connect the SUT to the impedance analyzer. The SUT must be placed into a quiet mode (non-transmitting). If possible, the detection circuitry which allows the SUT to detect the TL signal should be disabled. Measure the SUT's complex impedance, Z_T, from 1 kHz to 200 kHz. The return loss at each frequency shall be calculated as follows:

$$Return\ Loss(dB) = 20\log\left|\frac{Z_T+135}{Z_T-135}\right|$$

where Z_T is the SUT's measured complex impedance at each frequency.

Note 1: A return loss measurement unit (e.g., network analyzer) can also be used in place of an impedance analyzer provided that the instrument can produce return loss values that are close to the above equation.

Note 2: Repeat the measurement with sealing current source of 1 mA and 20 mA.

PASS-FAIL CRITERIA:
The SUT's return loss must be above the return loss specified in ANS T1.601-1988, figure 17. This figure is reproduced in figure 7 below.

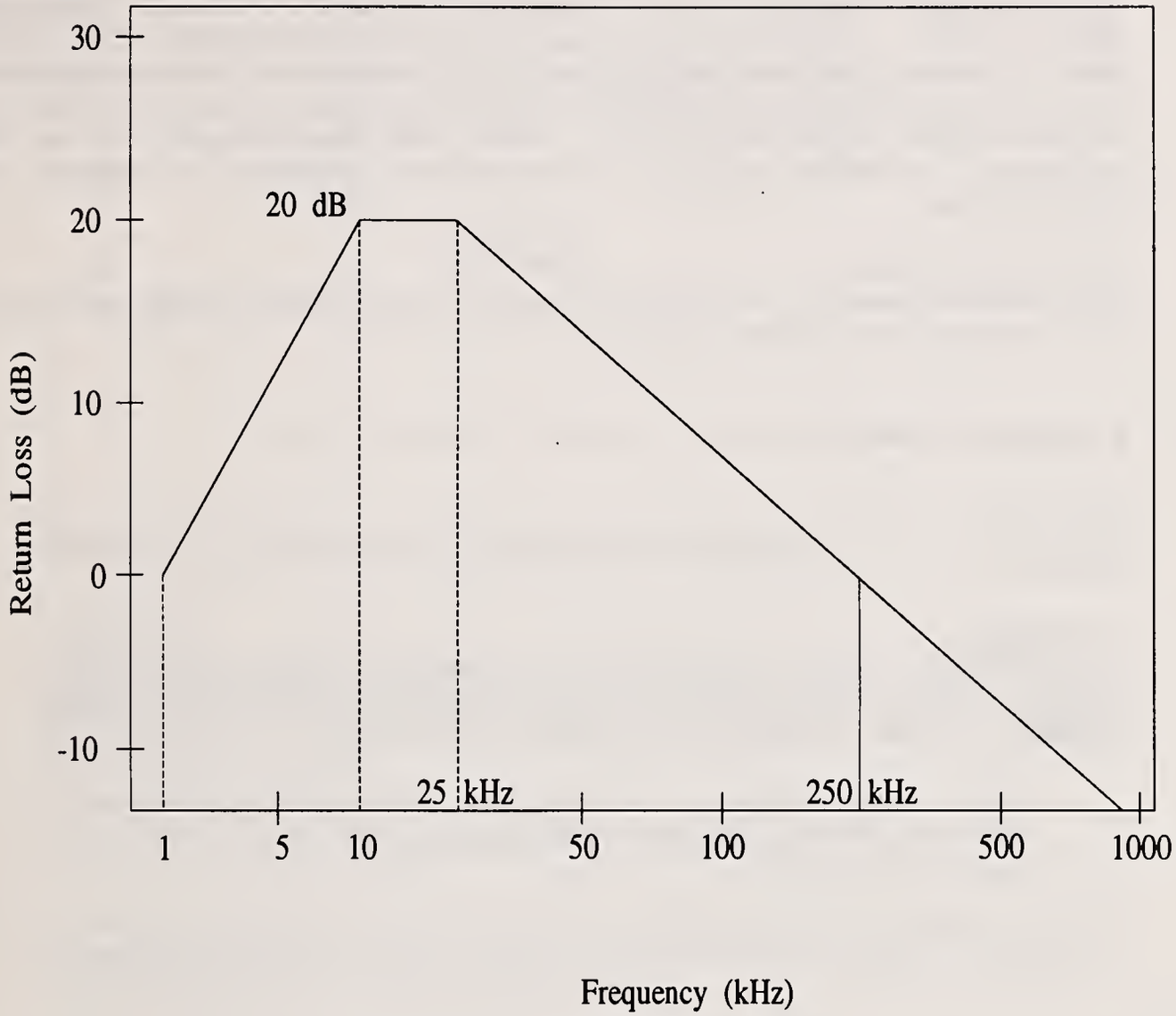


Figure 7. Minimum Return Loss.

4.2 Longitudinal Output Voltage Test

PURPOSE:
The purpose of this test is to measure the longitudinal component of the SUT's transmitted signal.

EQUIPMENT:
• Spectrum Analyzer with balanced input

CONFIGURATION:
ANS T1.601-1988, figure 18, shows the test configuration for the longitudinal output voltage test.

PROCEDURE:
This test shall be performed with the SUT continuously transmitting SN3 or equivalent signal in the absence of the received signal. The spectrum analyzer settings should be configured as follows: a 1 kHz resolution bandwidth (RBW), a -40 dBV reference level and a 30 Hz video bandwidth (VBW). Connect the SUT ground, if available, to the chassis ground of the spectrum analyzer as shown in the test configuration. By adjusting the center frequency of the spectrum analyzer in 1 kHz increments, measure the SUT's output longitudinal energy from 100 Hz to 270 kHz. At each center frequency record 1 s of rms voltage measurements. Perform an average on all of the recorded measurements for any four consecutive center frequency settings.

PASS-FAIL CRITERIA:
The results shall show less than -50 dBV over the frequency range of 100 Hz to 170 kHz, and less than -80 dBV over the range from 170 kHz to 270 kHz.

4.3 Longitudinal Balance

PURPOSE:
To verify that the SUT's longitudinal balance is within the limits specified in ANS T1.601-1988, section 7.3.

EQUIPMENT:
• variable frequency signal generator that is capable of supplying any frequency up to 160 kHz.
• frequency-selective voltmeter tuned to within 1 kHz resolution bandwidth of the signal generator frequency. The voltmeter used shall have balance of at least 70 dB.

> **Note:** Another alternative to measuring longitudinal balance can be found in NIU/ACT-1/89-026R5. The 100 ohm resistor shall be replaced with a 135 ohms in ANS T1.605-1989, figure 17 .

CONFIGURATION:

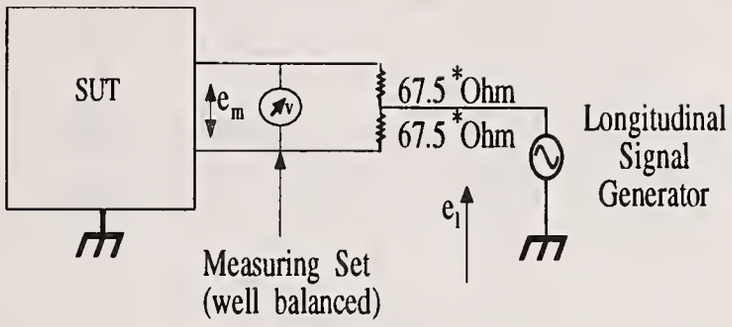


Figure 8. Measurement Method for Longitudinal Balance.

* These resistors need to be matched to better than 0.03% tolerance.

PROCEDURE:
At each frequency, the longitudinal signal, e_l, shall be applied as shown in figure 8. The longitudinal signal shall be at least 1 V rms. The corresponding metallic voltage, e_m, shall be measured across the 135-ohm termination provided by the test bridge. The SUT's longitudinal balance is computed as follows:

$$LongitudinalBalance = 20\log\left|\frac{e_l}{e_m}\right| dB.$$

To verify that the reading is caused by the SUT's imbalance and not by extraneous noise, the measurement shall be repeated with a change in the longitudinal source voltage, e_l, to produce a corresponding change in the measured metallic voltage, e_m.

PASS-FAIL CRITERIA:
The SUT's longitudinal balance shall be greater than 60 dB at frequencies below 4 kHz and greater than 55 dB for frequencies between 4 kHz and 160 kHz.

4.4 Jitter Limitations, NT Output

PURPOSE:
To verify that the SUT's transmitted signal conforms to the output jitter limitation specified in ANS T1.601-1988, section 7.4.2.

EQUIPMENT:
- Layer 1 tester capable of jittering its transmitted signal
- 12 bit waveform digitizer
- digital computer

CONFIGURATION:

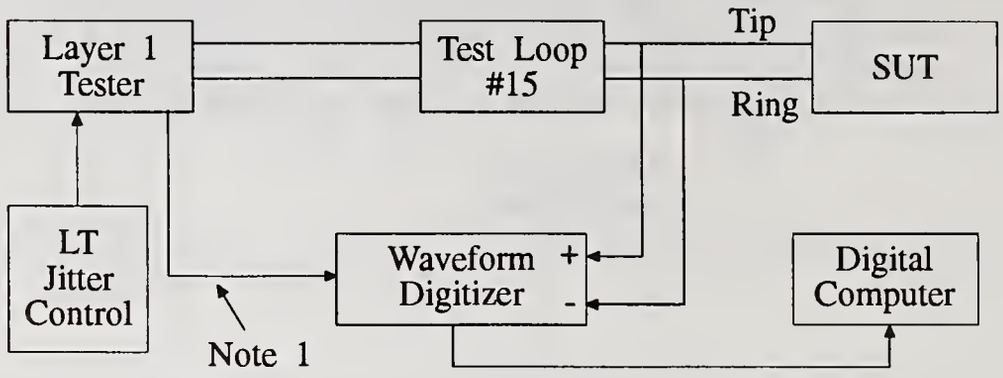


Figure 9. Configuration for Output Jitter Limitation Verification.

Note 1: Layer 1 tester 2B1Q transmitted signal, uncorrupted by the SUT 2B1Q signal.

Note 2: The digitizer's sampling frequency should be locked to the Layer 1 tester's baud rate.

PROCEDURE:
With the equipment connections shown in figure 9, the LT jitter control shall introduce jitter on the Layer 1 tester transmitted signal at discrete frequencies consistent with ANS T1.601-1988, figure 20. The LT jitter control shall introduce jitter on the Layer 1 tester's transmitted signal after full duplex transmission is achieved by both transceivers. When both transceivers have achieved transparency with LT jitter present, the SUT and Layer 1 tester outputs shall be captured by a waveform digitizer and transferred to a digital computer for software analysis (see app. C for details on jitter software processing). The waveform digitizer should sample the SUT's output signal at a minimum sampling rate of 4 samples/baud.

This process shall be repeated at the following frequencies and magnitudes:

Table 4.4.1. Jitter Magnitudes Vs. Test Frequencies

Frequency (Hz)	UI p-p*
0.5	0.3
1	0.15
2	0.075
5	0.03
10	0.015
19	0.008
83.33	0.008
100	0.008
500	0.008
666.67	0.008
1000	0.008

*1 UI (Unit Interval) = 1 symbol baud = 12.5μs

Note: LT jitter control also is employed for SUT performance testing of ANS T1.601-1988, section 5.4.2.

PASS-FAIL CRITERIA:
With the Layer 1 tester's transmitted signal jittered as previously described, the jitter on the SUT transmitted signal shall conform to the following:

1. The absolute jitter shall be equal to or less than 0.04 UI peak-to-peak and less than 0.01 UI rms when measured with a high-pass filter having a 6 dB/octave roll-off below 80Hz.

2. The relative jitter in the phase of the SUT transmitted signal shall not exceed 0.05 UI peak-to-peak and 0.015 UI rms when measured with a band-pass filter having 6 dB/octave roll-offs above 40 Hz and below 1.0 Hz. This applies for LT jitter frequencies up to 19 Hz.

3. The expression below must be observed for the maximum difference of the instantaneous SUT transmitted phase relative to instantaneous LT transmitted phase from the average difference between the SUT transmitted phase and LT transmitted phase shall not exceed 0.1 UI.

$$\max\left| \phi_{inst} - \phi_{longterm} \right| \leq 0.1 UI$$

Where:
ϕ_{inst} = instantaneous phase of SUT transmitted signal relative to SUT received signal. $\phi_{longterm}$ = long term ave. phase difference between SUT transmitted and received signals.

4.5 DC Characteristics Tests

4.5.1 Metallic Termination I-V Characteristics

PURPOSE:
The tests in this section check to see that the SUT uses a DC metallic termination with the proper I-V characteristics.

EQUIPMENT:
- autoranging power supply under computer control
- Voltmeter
- Ammeter

CONFIGURATION:

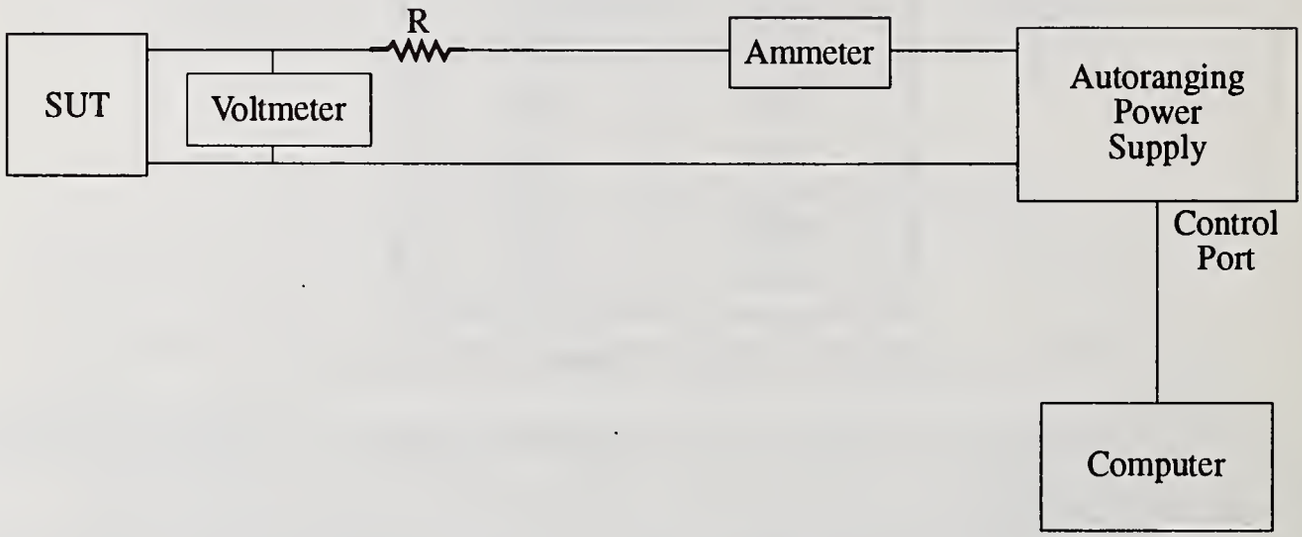


Figure 10. DC Termination Test.

PROCEDURE:
Figure 10 shows the test configuration for the DC metallic termination. An autoranging power supply is connected in series with a resistor and the SUT. A series of tests are performed to check the current-voltage characteristics of the metallic termination of the SUT. The maximum continuous voltage and maximum short-term voltages will be tested as well. These tests are performed under computer control over an instrumentation bus. Manual control is possible, but careful attention should be used when performing the maximum voltage short-term test. ANS T1.601-1988, figure F2 is a diagram of the DC characteristics of an acceptable line termination. The voltage and current values are subject to change as the standard evolves. All of the tests in this section are performed twice by reversing the polarity of the power supply voltage.

The first test uses a 200 ohm series resistor to check the current-voltage characteristics of the SUT's metallic termination. All stimulus of the power supply (voltage change or current change) will be held constant for at least 500 ms at which time the SUT's response will be checked (voltage or current measurement). Set the voltage at the SUT's termination to 20 V and read the DC leakage current (ILK). The off state leakage current (ILK) should be less than 5 μA. Adjust the voltage at the termination to 30 V (Non Active Voltage) and measure the current, which should be less then the breakover current threshold

of 0.15 mA (IBO). Raise the voltage at the termination to 39 V to test the maximum activate voltage threshold (VBO). Measure the on state current, which should be in the 25 (ILmin) to 70 mA (ILmax) range. Step the termination voltage up in one volt increments from 39 to 56 V and measure the continuous "ON" current. This current should also be in the range of 25 to 70 mA. Lower the termination voltage in one step decrements from 38 to 15 V and now measure the continuous "ON" current. This current should now be in the range of 20 mA (ITST) to 70 mA (ILmax). Adjust the series current down to 20 mA and measure the voltage at the SUT's termination. The dc voltage drop at 20 mA should be less than 15 V. Lower the series current to 1 mA by lowering the voltage at the termination. A 1 mA hold current (IHLD) should be achievable in the on state. Measure the voltage at the termination and record this voltage as VHLD (voltage at 1 mA hold current). This VHLD value will be used in the metallic transition time tests. Continue to lower the series current by decreasing the voltage. The termination should go into the off state (open) before 0.2 mA is reached. This is called the guaranteed release current (IRLS). The transition to the off state is determined by observing the decrease in current to a near-zero value (less than 5 μA).

The next test will be performed twice, once with a 200 ohm series resistor and once with a 4000 ohm series resistor. Adjust the power supply to 70 V for a test duration of 2 s. Measure the current at each half second interval. The series current at each half second interval should be between 7 mA and 70 mA.

PASS-FAIL CRITERIA:
The requirements for each test are noted in the PROCEDURE text. Also see ANS T1.601-1988, table 6.

4.5.2 Metallic Termination Transition Times

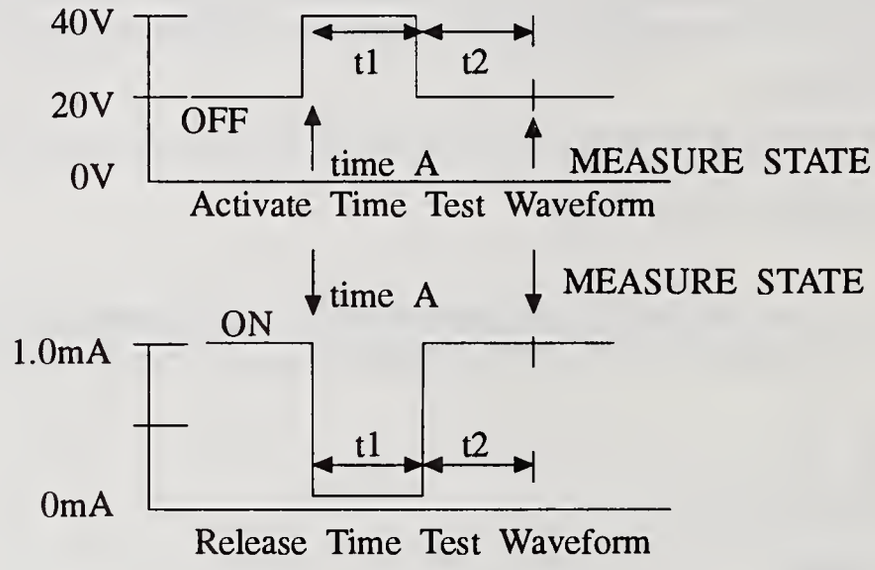
PURPOSE:
The tests in this section will verify proper implementation of the state transition times of the SUT's metallic termination. State transition time requirements from the off state to the on state and vice-versa will be verified.

EQUIPMENT:
The same as for section 4.5.1.

CONFIGURATION:
See figure 10 above.

PROCEDURE:
First the activate transition times will be checked using the same test configuration as above with a 200 ohm series resistor. In these activate tests, various time duration "turn on" voltages (≥39) at the termination will be applied followed by a 500 ms voltage of 20 V at the termination. Refer to figure 11 where the turn on time duration is t_1. The 500 ms of 20 V at the termination which follows t_1 is t_2 in figure 11. For this set of tests, the DC termination will be placed in the OFF state by applying 0 V for more than 500 ms followed by 20 V at the termination for more than 500 ms prior to the beginning of the application of the "turn on" voltage (time A). The state of the termination is verified to be in the OFF state prior to the beginning of the application of the "turn on" voltage by measuring the series current at time A. The termination should be OFF at time A by measuring a series current which is less than .15 mA. After the application of the "turn on" voltage, the series current is measured at the end of t_2 in order to determine if the DC termination transitioned to the ON state or not. The termination is considered to be ON if the series current is above 20 mA (ITST). The termination is considered to be OFF if the series current is less than 0.15 mA. The first set of activate checks should be performed with a value of t_1 which is less than 10 ms. The termination should be OFF when its state is checked at the end of t_2. The next set of tests should be performed with the value of t_1 which is greater than 50 ms. Now the state of the termination should be ON when it is checked at the end of t_2.

The release state transition times will be verified in a similiar as the activate times. The release time waveform is provided in figure 11. These tests will be performed by first placing the SUT's termination into the ON state. This should be achieved by applying 40 V at the SUT's termination for at least 500 ms. The SUT will then be brought to the hold current state by lowering the series current to 1 mA for at least 500 ms (time A). This can be achieved by adjusting the voltage at the NT's termination to the VHLD value recorded in the DC characteristics test. The release time tests will be conducted by removing any series current by setting the voltage output to zero for the time duration indicated by t_1. After the removal of the series current for t_1 time duration, attempt to create a series current of 1 mA by setting the voltage at the SUT's termination to the recorded VHLD value. This voltage should be applied for 500 ms, at which time the state of the SUT's termination is checked. If the series current is less than 0.15 mA, the termination is in the OFF state. If the series current is equal to 1 mA then the termination is in the ON state. The first release time test to be performed should be conducted with the value of t_1 set to less than 10 ms. The resultant state of this test should indicate that the SUT's termination is in the ON state. The last set of tests to be performed is to set the value of t_1 to be greater than 50 ms. The results of these tests should show that the SUT's termination is in the OFF state.



Change of state shall not occur if $t_1 \leq 10$ msec
Change of state shall not occur if $t_1 \leq 5$ msec
$t_2 = 500$ msec

Figure 11. Metallic Termination Transition Times.

PASS-FAIL CRITERIA:
The requirement for each portion of the test is indicated in the PROCEDURE text above.

4.5.3 Sealing Current Tests

PURPOSE:
To verify that the SUT performs normally with sealing current applied in the range of 1.0 mA to 20 mA.

PROCEDURE:
During the impedance and return loss measurement described in section 4.1 of this document, various sealing currents are applied.

Repeat the performance tests described in section 3.5 of this document using loop #15 while applying sealing currents of 1.0 mA, 10 mA, and 20 mA.

PASS-FAIL CRITERIA:
The SUT must pass the requirements stated in sections 3.5 and 4.1 of this document while the specified sealing currents are applied.

5 FUNCTIONAL CHARACTERISTICS

5.1 Baud Rate, Timing & Synchronization

PURPOSE:
To verify that the SUT can operate with the received signal baud rate in the range of 80 kbaud ±5 ppm (from 79999.6 baud to 80000.4 baud) or 80 kbaud ±32 ppm if the NT is designed to operate with other equipment as specified in ANS T1.601-1988, section 6.1.

EQUIPMENT:
- Layer 1 tester with an adjustable clock offset
- an analog scope

CONFIGURATION:

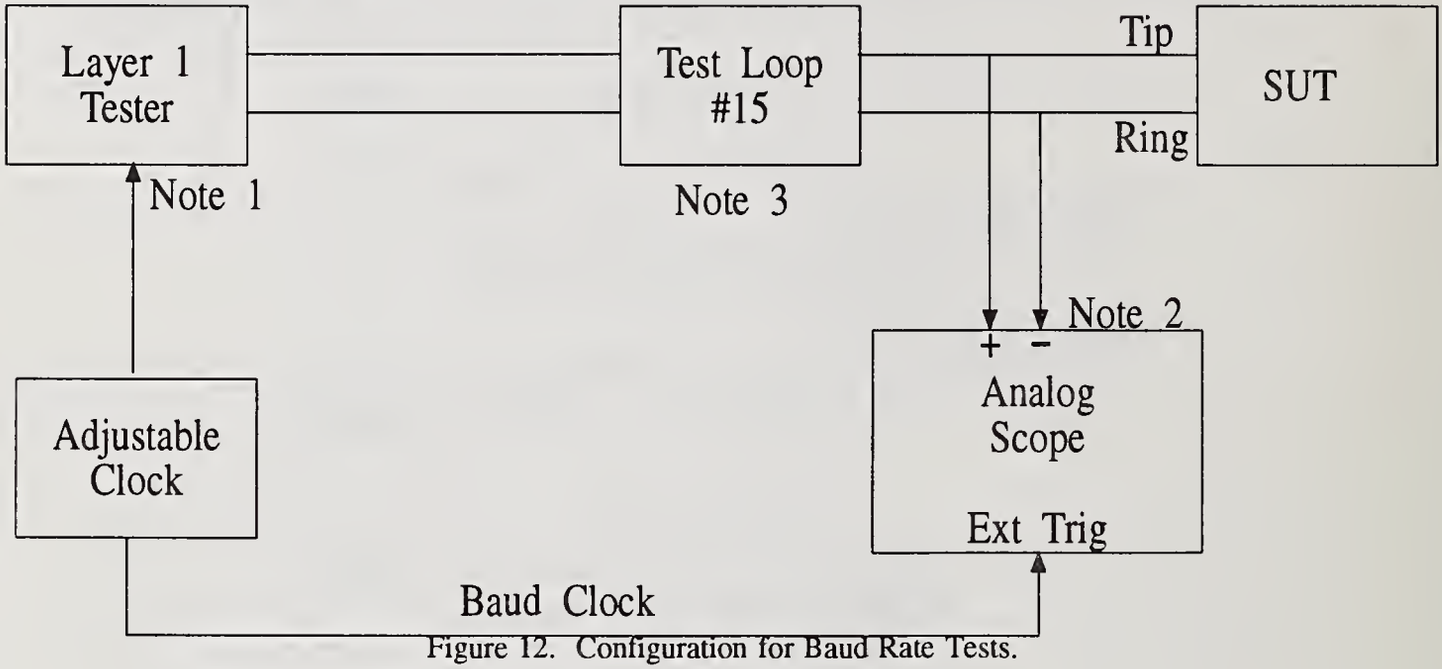


Figure 12. Configuration for Baud Rate Tests.

Note 1: A high rate clock from which the baud timing is derived should be used.

Note 2: High impedance differential probe.

Note 3: Loop #15 was selected because it is the simplest loop over which to establish the required full duplex transmission and transparency.

PROCEDURE:
The equipment should be connected as shown in figure 12. In order to verify baud rate, timing and synchronization, full duplex transmission and transparency must be established. Thus, loop 15 is used to establish full duplex transmission and transparency since this is the shortest loop from the 15 test loops. The Layer 1 tester must be able to send 2B1Q bitstreams toward the SUT at variable baud rates between 79999.6 and 80000.4 baud. The analog oscilloscope must be adjusted to trigger on a baud clock. If the oscilloscope display does not drift, the SUT's transmit baud rate is the same as that of the Layer 1 tester. If the Layer 1 tester baud rate is changed, the same procedure must be repeated to determine the SUT's ability to synchronize to the received signal. The Layer 1 tester baud rate must be set at 79999.6, 79999.8, 80000.0, 80000.2, and 80000.4 baud. The SUT transmit signal must be observed for at least 5 min and

remains locked to the Layer 1 tester signal for the entire observed interval (e.g., momentary synchronization failure is not permitted). For the two extreme baud rates (79999.6 and 80000.4 baud), the observed interval shall be at least 10 min.

For NT implementations intended for other applications in addition to providing network access; such as behind an NT2; e.g., PBX; or other piece of network equipment operating in stand-alone mode, the procedure above should be used. These NTs should be designed to operate with a received signal having a maximum tolerance of ±32 ppm (or ±2.56 baud). Therefore, the Layer 1 tester baud rate should be set at 79997.44, 79998.4, 79999.6, 80000.4, 80001.6, and 80002.56 baud.

Note: To avoid verifying the SUT's ability to synchronize to the Layer 1 tester baud rate at different frequencies, the Layer 1 tester can provide baud rate that produces maximum allowable frequency offset relative to the measured SUT's free-running baud rate. If the SUT passes this condition, it is considered compliant and the procedure does not have to be repeated at other baud rates.

PASS-FAIL CRITERIA:
The SUT shall extract baud timing for its transmit signal from the received signal provided by the Layer 1 tester. As the NT received signal varies between 79999.6 and 80000.4 baud, the SUT transmit baud rate shall also be between 79999.6 and 80000.4 baud, and shall remain locked to the Layer 1 tester signal.

For NTs intended for other applications, in addition to providing network access, the SUT transmit baud rate should be between 80 kbaud ± 32 ppm.

Note: For NTs implementations intended for other applications, in addition to providing network access, it is only necessary to perform one test with Layer 1 tester baud rate varying between 79997.44 baud and 80002.56 baud.

5.2 Start-up Procedures

5.2.1 Start-Up Sequence

PURPOSE:
To verify whether the SUT satisfies the start up sequence as described in ANS T1.601-1988, section 6.4.6.

EQUIPMENT:
- Layer 1 tester
- Digital Storage Device (Digitizing scope/Waveform Recorder)
- Time Interval counter
- Loop Simulator

Note: All test suites in sections 5.2.1 through 5.2.4 of this document use the same equipment as listed above and will not be repeated hereafter.

5.2.1.1 Activation from Customer Equipment

CONFIGURATION:

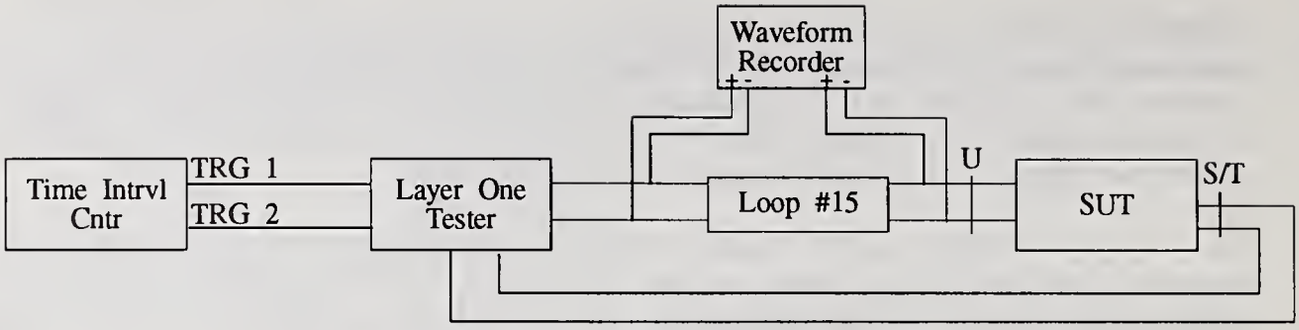


Figure 13. Configuration for Activation Tests.

Note: The Layer 1 tester's baud rate shall be adjusted to produce the maximum allowable frequency offset (80 kbaud ±5 ppm) relative to the SUT's free-running baud rate.

PROCEDURE:
Connect the SUT to a Layer 1 tester as shown in figure 13. Ensure that the SUT is in the cold start/RESET state. The Layer 1 tester will emulate an LT and respond to the SUT's start-up sequence with the appropriate signals (i.e., TL, SL1, SL2). If the S/T interface is present, INFO 1 signal may be provided by the Layer 1 tester to activate the NT start-up process. Alternately, the SUT can equip itself with the ability to initiate activation. The Layer 1 tester shall start the time interval counter upon detection of the TN signal (trigger 1), and stop the counter upon detection of a full operational status indicator (trigger 2). This indicator may be provided by the SUT. If the S/T interface is present, the INFO 2 signal may be used as an indication that the SUT is in full operation. Alternately, the Layer 1 tester can also detect the presence of the ISW and use that as an indication to the SUT's full operational status.

It is recommended that two LT start-up sequences be used to measure the SUT's activation time. The first sequence shall use all start-up signals (TL, SL1, SL2, SL3). The second sequence should omit the SL1 signal because this signal is optional.

PASS-FAIL CRITERIA:
The SUT shall respond with the TN signal upon detection of a request for start-up from customer equipment. The SUT shall be in full operation within 5 s (excluding the LT training period).

5.2.1.2 Activation from the Network

CONFIGURATION:
See figure 13.

PROCEDURE:
Connect the SUT to a Layer 1 tester as shown in figure 13. Ensure that the SUT is in the cold start/RESET state. The Layer 1 tester will emulate an LT and provide the start-up signals (TL, SL1, SL2) to activate the SUT.

To verify the SUT's ability to respond with TN signal within 4 ms from the beginning of TL signal, the Layer 1 tester shall configure the waveform digitizer so that both channels trigger at the start of the LT signal (i.e., one channel records the LT signal and the other channel records the TN signal). The time difference between the trigger points of the two recorded signals is the SUT's response time to the TL signal.

To verify the SUT's ability to start-up within 5 s, the Layer 1 tester shall start the time interval counter upon the start of the wake up tone TN (trigger 1), and stop the counter upon detection of a full operational status indicator (trigger 2). This indicator may be provided by the SUT. If the S/T interface is present, INFO 2 signal may be used as an indication that the SUT is in full operation. Alternately, the Layer 1 tester can also detect the presence of the ISW and use that as an indication to the SUT's full operational status.

It is recommended that two LT start-up sequences be used to measure the SUT's activation time. The first sequence shall use all start-up signals (TL, SL1, SL2, SL3). The second sequence should omit the SL1 signal because this signal is optional.

PASS-FAIL CRITERIA:
The SUT shall respond with the TN signal within 4 ms from the beginning of the TL signal. The SUT shall be in full operation within 5 s (excluding the LT training period).

5.2.1.3 Deactivation

CONFIGURATION:

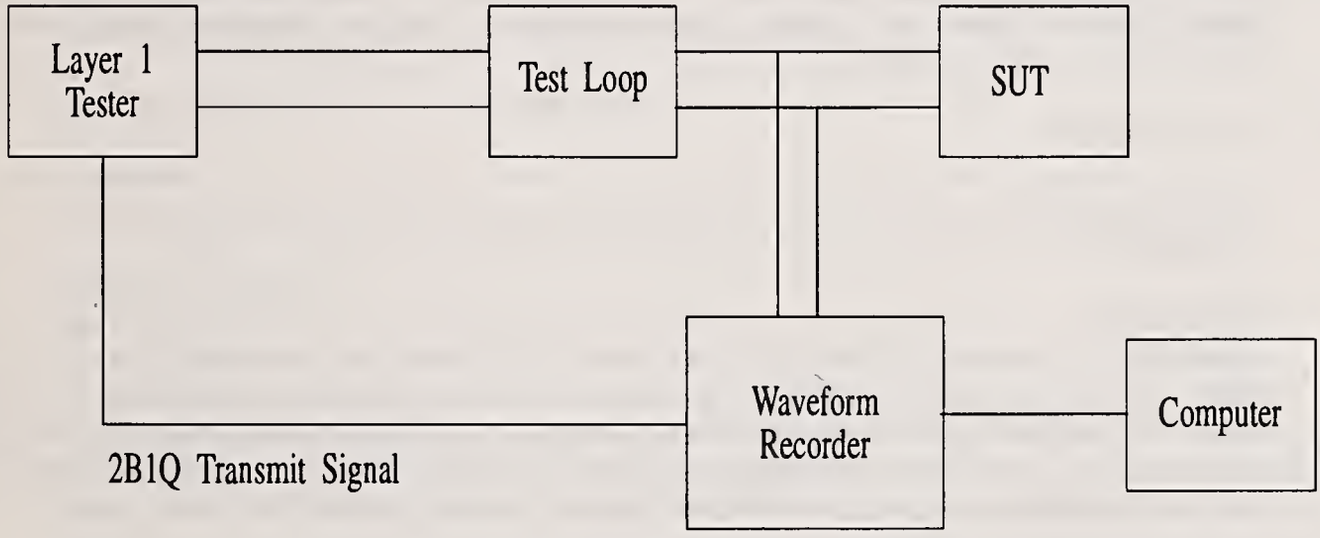


Figure 14. Configuration for Various Start-Up Tests.

PROCEDURE:
Connect the equipment as shown in figure 14. Ensure that the SUT is in cold start/RESET state. The Layer 1 tester will initiate start-up by sending the TL signal toward the SUT. After both transceivers are in full operation, the Layer 1 tester shall announce deactivation by setting dea = 0. The Layer 1 tester shall continuously send the SL3 signal with dea = 0. The Layer 1 tester must monitor the SUT's output signal to verify that it is still sending the SN3 signal. After verifying that the SUT is still active, the Layer 1 tester then ceases transmission (i.e., SL0). The Layer 1 tester must verify that the SUT enters the RECEIVE RESET state within 40 ms (i.e., SN0) upon the occurrence of the transition to no signal at its interface.

The above procedure should be repeated with the Layer 1 tester sending the minimum number (3) of dea = 0 bits before ceasing transmission.

PASS-FAIL CRITERIA:
The SUT's response time to a loss of received signal after detecting dea = 0 in at least three consecutive frames shall be less than 40 ms.

5.2.2 Signals During Start-Up

This section provides test suites to verify signals during start-up as defined in ANS T1.601-1988, section 6.4.4 and table 5.

5.2.2.1 Verify Signal TN/SN1 and Synchronization Word

CONFIGURATION:
See figure 14.

PROCEDURE:
Connect the SUT as shown in figure 14. Ensure that the SUT is in the cold start/RESET state. The Layer 1 tester will initiate start-up by sending the TL signal. The SUT's response (TN and SN1) to the Layer 1 tester activation request shall be captured. With the exception of the TN signal (10-kHz tone), the captured SN1 signal shall be decoded, descrambled and deframed before searching for the correct data pattern as defined in ANS T1.601-1988, table 5.

PASS-FAIL CRITERIA:
The SUT shall transmit a 10-kHz TN tone for 6 frames and shall consist of four +3 symbols and four -3 symbols. The SN1 signal shall contain synchronization words (SW), no superframe marker (ISW), and 2B+D and M bits set to binary ones.

5.2.2.2 Verify Signal SN2

CONFIGURATION:
See figure 14.

PROCEDURE:
Connect the SUT as shown in figure 14. Ensure that the SUT is in the cold start/RESET state. The Layer 1 tester will initiate start-up by sending the TL signal. The Layer 1 tester must respond with SL1 (or SL2 if SL1 is omitted) within 480 ms after detecting cessation of signal TN (or SN1 if it is sent). The SUT's response to SL2 signal shall be captured. The Layer 1 tester shall decode, descramble and deframe the signal SN2 before searching for the correct data pattern as defined in ANS T1.601-1988, table 5.

PASS-FAIL CRITERIA:
The SN2 signal shall contain synchronization words (SW), no superframe marker (ISW), and 2B+D and M bits set to binary ones with frame offset at 60 ±2 quaternary symbols.

5.2.2.3 Verify Signal SN3

Section 5.5 provides a procedure to verify User Data (2B+D). The signal SN3 is verified in section 5.5 of this document. Therefore, it is unnecessary to verify the signal SN3 separately.

5.2.3 Timers

This section is devoted to ANS T1.601-1988, section 6.4.3 (Timers). Four failure conditions will be created to verify the SUT's response as specified in ANS T1.601-1988, section 6.4.3. The first three conditions (i.e., failure to complete start-up, loss of received signal, loss of synchronization) are described as conditions (1), (2), and (3) in ANS T1.601-1988, section 6.4.3. The fourth condition is described in figure 16 and table 5 (between time T2 and T3) and in the last paragraph of ANS T1.601-1988, section 6.4.3.

5.2.3.1 Failure to Complete Start-Up Within 15 Seconds

PURPOSE:
To verify the SUT's ability to function as specified in ANS T1.601-1988, section 6.4.3.

CONFIGURATION:
See figure 14.

PROCEDURE:
Connect the equipment as shown in figure 14. Ensure that the SUT is in the cold start/RESET state. The Layer 1 tester should initiate start-up by sending TL tone. The SUT must respond with TN and/or SN1 signals (this must also be verified by the Layer 1 tester, see sec.5.2.2.1). Upon detection of cessation of signal TN (or SN1 if it is sent), the Layer 1 tester then starts sending SL2 containing corrupted SW/ISW for a period of 15 s. After the 15 s period expires, the Layer 1 tester resume sending the normal SL2 signal (i.e., stops corrupting SW/ISW). The SUT's output signal must be monitored for at least 15 s. The SUT's response to a failure to start-up within 15 s shall be the SN0 signal (i.e., the 0 V signal).

PASS-FAIL CRITERIA:
Upon failure to complete start-up within 15 s, the SUT must cease transmission and then, upon the subsequent detection of the loss of received signal, it shall enter the RECEIVE RESET state.

5.2.3.2 Loss of Received Signal for more than 480 ms

PURPOSE:
To verify the SUT's ability to function as specified in ANS T1.601-1988, section 6.4.3.

CONFIGURATION:
See figure 14.

PROCEDURE:
To verify the SUT's ability to enter the RECEIVE RESET immediately when loss of received signal is detected for more than 480 ms, the Layer 1 tester must first initiate start-up to establish full operational status in both transceivers (i.e., state H8 in ANS T1.601-1988, table C1). Once full duplex is established, the Layer 1 tester then stops transmitting the SL3 signal toward the SUT. The Layer 1 tester must continuously monitor the SUT's response to loss of received signal, verifying that normal SN3 transmission occurs for at least 480 ms. The Layer 1 tester shall start the 40 ms time interval counter when the SUT stops sending signal toward the Layer 1 tester. This signifies that the SUT is in the RECEIVE RESET state. Two tests must be performed to monitor the SUT's behavior while it is in the RECEIVE RESET state:

1. Within 40 ms after the SUT enters the RECEIVE RESET state, the Layer 1 tester shall send wake-up tone TL to initiate start-up again. The purpose of sending the TL tone again is to verify that the SUT is capable of responding to wake-up tone while in the RECEIVE RESET state. After sending wake-up tone TL, the Layer 1 tester shall be ready to capture the received signal to verify that the SUT actually responds to TL with the TN signal.

2. The Layer 1 tester shall not send any signal toward the SUT for at least 40 ms while the SUT is in the RECEIVE RESET state. The Layer 1 tester must continuously monitor the SUT and verify that the SUT does not send any signal (i.e., SN0) during the 40 ms interval.

Note: Although loss of received signal is not defined in ANS T1.601-1988, it is assumed to be the 0 V signal (SL0). This SL0 signal shall not be interpreted as any other signal (e.g., SL3). Falsely identifying

the SL0 signal could possibly put the SUT into other states that are not defined in ANS T1.601-1988, section 6.4.3. If the SUT does not enter the RECEIVE RESET state (state H12 in ANS T1.601-1988, table C1) after the 480 ms time interval expired, it will be considered as non-compliant.

PASS-FAIL CRITERIA:
Upon detection of loss of received signal for more than 480 ms, the SUT must enter the RECEIVE RESET state. The SUT shall remain in the RECEIVE RESET state for at least 40 ms and is not permitted to initiate the start-up sequence but shall be capable of responding to the initiation of start-up sequence by the Layer 1 tester.

5.2.3.3 Loss of Synchronization for more than 480 ms

PURPOSE:
To verify the SUT's ability to function as specified in ANS T1.601-1988, section 6.4.3.

CONFIGURATION:
See figure 14.

PROCEDURE:
To verify the SUT's ability to respond correctly when loss of synchronization occurs for more than 480 ms, the Layer 1 tester will first initiate start-up (sending TL signal) to establish full operational status in both transceivers (i.e., state H8 in ANS T1.601-1988, table C1). The Layer 1 tester then starts transmitting superframes containing corrupted SW/ISWs. The Layer 1 tester must continuously monitor the SUT's response, verifying that normal SN3 transmission occurs for at least 480 ms after the start of the corrupted LT frames. Upon being in loss of synchronization state for greater than 480 ms the SUT shall cease transmission. When the Layer 1 tester detects that the SUT stops transmitting SN3 signal (i.e., loss of received signal for more than 480 ms), the Layer 1 tester then ceases its SL3 signal. Within 40 ms after detection of the loss of signal from the Layer 1 tester, the SUT shall enter the RECEIVE RESET state. The Layer 1 tester must continuously monitor the SUT's response to loss of received signal at the end of the 480 ms time interval.

Because the SUT is allowed up to 40 ms to enter the RECEIVE RESET state after the Layer 1 tester ceases transmission, it is very difficult to determine when the SUT is actually in the RECEIVE RESET state. Therefore, testing the SUT's behaviors while in the RECEIVE RESET state is not performed here. However, the SUT must pass the tests described in section 5.2.3.2 of this document.

PASS-FAIL CRITERIA:
When loss of synchronization occurs for more than 480 ms, the SUT must cease transmission and then, upon the subsequent detection of the loss of received signal within 40 ms, it shall enter the RECEIVE RESET state.

5.2.3.4 Verify Proper State if no Signal is Received upon Cessation of TN

PURPOSE:
To verify the SUT's ability to enter the FULL RESET state when no signal is received within 480 ms after it ceases sending signal TN or SN1 if it is sent (ANS T1.601-1988, sec. 6.4.3 and fig. 16).

CONFIGURATION:
See figure 14.

PROCEDURE:
To verify the SUT's ability to enter the FULL RESET state when no signal is received within 480 ms after it ceases sending TN or SN1, connect the equipment as shown in figure 14. Ensure that the SUT is in cold start/RESET state. The Layer 1 tester will initiate start-up by sending wake-up tone TL toward the SUT. The SUT must respond with TN (this must also be verified by the Layer 1 tester, sec.5.2.2.1 of this document). Upon detection of cessation of signal TN (or SN1 if it is sent), the Layer 1 tester then remains quiet (not sending signal SL1 or SL2 if SL1 is omitted) for more than 480 ms. When the 480 ms time interval expires, the Layer 1 tester resumes sending the SL1 or SL2 signal. The Layer 1 tester must verify that the SUT enters the FULL RESET state. That is, the SUT stops sending signal toward the Layer 1 tester.

PASS-FAIL CRITERIA:
The SUT must enter the FULL RESET state if signal SL1 or SL2 is not detected within 480 ms after it ceases transmitting TN/SN1.

5.2.4 Verify Warm Start Activation

PURPOSE:
To verify that the SUT meets the requirements for warm starts as defined in ANS T1.601-1988, section 6.4.7 and figure 16.

CONFIGURATION:
See figure 14.

PROCEDURE:
Activate the SUT using the cold start activation procedures. Monitor the Cold Start Only (cso) bit in the superframe transmitted by the SUT. If cso = 1, the SUT does not implement warm start activation; discontinue the test. If cso = 0, send a deactivate request (dea=0) in three consecutive superframes from the Layer 1 tester and immediately cease transmission following the third superframe. The SUT, upon detection of loss of signal, shall cease transmission. Using the same procedure as outlined in 5.2.1 above, measure the time required to achieve full operational status. Using the storage device, measure the time between TN/SN1 cessation and SL1 initiation.

Note: The Layer 1 tester's baud rate shall be adjusted to produce the maximum allowable frequency offset (80 kbaud ±5 ppm) or 80 kbaud ± 32 ppm if the SUT is designed for other applications.

PASS-FAIL CRITERIA:
The time recorded by the interval counter minus both the time that SL1 is present and the time between TN/SN1 and SL1 must be less than or equal to 150 ms, as defined in ANS T1.601-1988, section 6.4.7 and figure 16.

Note: Warm start capability is optional, but if the option is not implemented the cso bit must be set to 1.

5.3 Frame Offset

PURPOSE:
To verify that the SUT meets the frame offset requirements outlined in ANS T1.605-1989, section 6.2.4.

EQUIPMENT:
• Dual trace waveform storage device

CONFIGURATION:
See figure 14.

PROCEDURE:
Capture both the transmitted and received waveforms as shown in figure 14. Using the ISW as a reference, measure the frame offset.

PASS-FAIL CRITERIA:
The offset between the received and transmitted frames must be between 0.725 ms and 0.775 ms.

5.4 Wiring Polarity

PURPOSE:
To verify that the SUT works with both normal and reverse polarity.

EQUIPMENT:
See section 5.2.1.

CONFIGURATION:
See figure 13.

PROCEDURE:
Repeat the test procedures described in section 5.2.1 of this document with tip and ring reversed and make sure that the start-up procedure follows correctly.

PASS-FAIL CRITERIA:
The SUT shall pass the pass-fail criteria described in section 5.2.1 of this document both in normal and reverse polarity.

5.5 User Data (2B+D)

PURPOSE:
To verify that the user data (2B+D) generated by the SUT is in compliance with requirements specified in ANS T1.601-1988, section 6.2.2.

EQUIPMENT:
• Layer 1 tester
• 12-bit waveform digitizer
• digital computer

CONFIGURATION:

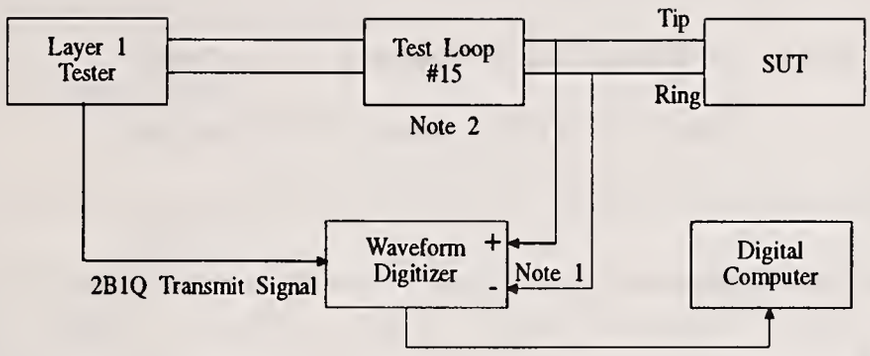


Figure 15. Configuration for User Data Test.

Note 1: High impedance, differential probe.

Note 2: Loop #15 was selected because it is the simplest loop over which to establish the required full duplex transmission and transparency.

PROCEDURE:
The equipment shall be connected as shown in figure 15. After both transceivers have achieved full duplex transmission and transparency, the SUT output signal shall be captured by a waveform digitizer. A minimum of 80 basic frames (or 120 ms) must be captured to ensure correct detection of the SW/ISW. The transmitted symbols (quats) must be extracted from the captured waveform. The following algorithm may be used to verify SUT's 2B+D data:

1. Reset basic frame counter to 0.

2. Search for the synchronization word (SW/ISW).

3. The next 108 symbols are allocated to the B1, B2, and D channels.

4. The following 3 symbols after the 2B+D data field are allocated to the M channel. These 3 symbols signify the end of a basic frame.

5. If the SW/ISW is identified immediately after step 4 above, increase the number of basic frames found by one since the beginning of each basic frame is marked by the SW/ISW. If the SW/ISW can not be located immediately after step 4 above, go back to step 1.

6. Repeat steps 2 to 5 until at least one superframe (8 basic frames) is located.

To test the SUT transmitter, the SUT must send a known binary data pattern (the SUT binary data pattern must be other than all ONEs or ZEROs, preferably an asymmetric pattern such as {1110 1001}), and the Layer 1 tester receiver will decode, descramble, and deframe the received data. The Layer 1 tester's received binary data and the SUT's transmit data must be the same.

PASS-FAIL CRITERIA:
If one superframe (8 basic frames) is located, the SUT data field allocation is correct. Following the synchronization word (9 symbols), the next 108 symbols in a basic frame shall be as shown in the table 5.5.1 below.

Except during start up, the channels shall be transparent to user data bits.

Table 5.5.1. 2B1Q Encoding of 2B+D Bit Fields

Data	Time → B_1				B_2				D
Bit Pairs	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (rel)	q_1	q_2	q_3	q_4	q_5	q_6	q_7	q_8	q_9
No. of Bits	8				8				2
No. of Quats	4				4				1

Where:

b_{11} = first bit of B_1 octet as received at the S/T interface
b_{18} = last bit of B_1 octet as received at the S/T interface
b_{21} = first bit of B_2 octet as received at the S/T interface
b_{28} = last bit of B_2 octet as received at the S/T interface
d_1d_2 = consecutive D-channel bits (d_1 is first bit of pair as received at the S/T interface)
q_1 = ith quat relative to start of given 18-bit 2B+D data field

Note: There are 12 2B+D 18-bit fields per 1.5 ms basic frame.

5.6 Scrambling

PURPOSE:
To check for proper operation of the scrambler according to ANS T1.601-1988, section 6.3.

PROCEDURE:
There is no specific test procedure for this feature. If the SUT passed the performance tests described in section 3.5 of this document, the scrambler is operating properly.

6 M-CHANNEL BIT FUNCTIONS

The following tests require the Layer 1 tester to provide capabilities for performing M-channel tests. This includes the capability of setting the M-channel bits to various values in the LT mode and also monitoring the M-channel bits transmitted by the SUT.

6.1 Cyclic Redundancy Check

PURPOSE:
To verify the correct implementation of the SUT's crc generator in accordance with ANS T1.601-1988, section 8.1.

EQUIPMENT:
Same as for section 5.5.

CONFIGURATION:
See figure 15.

PROCEDURE:
Connect the SUT to the Layer 1 tester as shown in figure 15. Allow the Layer 1 tester and the SUT to activate into sending normal operating signals (SL3 and SN3). Set the Layer 1 tester to send a PRBS (Pseudo-Random Bit Stream) in the 2B+D channels. Have the Layer 1 tester continuously monitor for crc errors in the transmit superframe of the SUT.

PASS-FAIL CRITERIA:
The SUT shall not produce any errors in generating the crc.

6.2 Far End Block Error (febe) Bit

PURPOSE:
To verify the correct implementation of the SUT's febe bit in accordance with ANS T1.601-1988, section 8.2.1.

EQUIPMENT:
Same as for section 5.5.

CONFIGURATION:
See figure 15.

PROCEDURE:
Connect the SUT to the Layer 1 tester as shown in the figure 15. Allow the Layer 1 tester and the SUT to activate into sending normal operating signals (SL3 and SN3). Set the Layer 1 tester to send a PRBS (Pseudo-Random Bit Stream) in the 2B+D channels. Using the Layer 1 tester's capability for monitoring the febe bit of the SUT, check to see that it is consistently set to a binary 1. If it is not consistently set to one, then the SUT has set the febe bit to the wrong binary value. Have the Layer 1 tester transmit superframes with corrupted crcs. Now monitor the febe bit of the SUT and verify that it is consistently set to a binary zero. If it is not set to zero, then the SUT has problems detecting crc errors.

PASS-FAIL CRITERIA:
The SUT shall set the febe bit to a binary zero in the next outgoing superframe upon detection of a block error in a received superframe.

6.3 Activation Bit

PURPOSE:
To verify the correct implementation of the SUT's act bit is in accordance with ANS T1.601-1988, section 8.2.2.

EQUIPMENT:
- Layer 1 tester
- Digital Storage Device (Digitizing scope/Waveform Recorder)
- Loop Simulator

CONFIGURATION:
See figure 13.

PROCEDURE:
Configure the SUT as shown in figure 13. Allow the Layer 1 tester and the SUT to go through a cold start activation sequence with the Layer 1 tester transmitting INFO 0 at the S/T interface. Once the SUT is sending SN3 and the Layer 1 tester is transmitting SL3 with its act bit set to a binary 0, monitor the act bit of the SUT. The act bit should be set to a binary 0. Have the Layer 1 tester transmit INFO 3 on the S/T interface. The value of the act bit should now be set to 1. Repeat this test again with the act bit of the Layer 1 tester set to a binary 1. Have the Layer 1 tester transmit data frames on the B and D channels over the S/T interface after the Layer 1 tester receives INFO4. The Layer 1 tester must monitor the SUT;s signal to verify that the S/T data is being passed on properly

PASS-FAIL CRITERIA:
The act bit of the SUT shall reflect its layer-2 readiness.

6.4 Power Status Tests

PURPOSE:
To verify the correct implementation of the SUT's power status bits in accordance with ANS T1.601-1988, section 8.2.4.

EQUIPMENT:
Same as for section 5.5.

CONFIGURATION:
See figure 15.

PROCEDURE:
Configure the SUT as shown in figure 15. To verify that the SUT implements the power status bits properly, the ps1 and ps2 bits will be monitored when the SUT is placed under various power conditions. First, let the LT and SUT fully activate by powering the SUT from its primary source. In this condition, which is normal operation, the ps1 and ps2 shall be set to one. Now remove the primary power from the SUT and monitor the SUT's response. If the SUT has a secondary power source (backup battery), the SUT shall set its ps1=0 and ps2=1. If the SUT doesn't support a secondary supply the SUT shall be able to indicate a "dying gasp" in at least 3 consecutive superframes. Both ps1 and ps2 shall be set to 0. If a secondary source is supported, perform the following test: remove the secondary source from the SUT, while leaving the primary source connected. The SUT shall indicate a secondary power out by setting ps1=1 and ps2=0. Now remove both the primary and secondary power sources from the SUT. The SUT shall be able to indicate a "dying gasp" in at least 3 consecutive superframes.

PASS-FAIL CRITERIA:
The SUT shall set its ps1 and ps2 to the values provided in ANS T1.601-1988, Table 7 when placed under various power conditions.

6.5 NT Test Mode Indicator

PURPOSE:
To verify the correct implementation of the SUT's ntm indicator bit in accordance with ANS T1.601-1988, section 8.2.4.

EQUIPMENT:
Same as for section 5.5.

CONFIGURATION:
See figure 15.

PROCEDURE:
Configure the SUT as shown in the figure 15. Allow the Layer 1 tester and the SUT to activate into sending normal operating signals (SL3 and SN3). Have the Layer 1 tester monitor the ntm indicator bit transmitted by the SUT. Under normal conditions the ntm bit shall be set to one. Place the SUT in a customer initiated test mode if this feature is supported by the SUT. Again have the Layer 1 tester monitor the ntm bit transmitted by the SUT. Now, the ntm bit shall be set to zero.

PASS-FAIL CRITERIA:
The ntm bit shall be a binary one in normal operation or a binary 0 when the SUT is in a customer initiated test mode.

6.6 Reserved Bits

PURPOSE:
To verify the correct implementation of the SUT's reserve bits in accordance with ANS T1.601-1988, section 8.2.7.

EQUIPMENT:
Same as for section 5.5.

CONFIGURATION:
See figure 15.

PROCEDURE:
Configure the SUT as shown in figure 15. Allow the Layer 1 tester and the SUT to activate into sending normal operating signals (SL3 and SN3). Have the Layer 1 tester monitor the reserve bits transmitted by the SUT. The reserve bits are the M4, M5 and M6 bits which have not been assigned by the standard.

PASS-FAIL CRITERIA:
The reserve bits shall always be set to a binary 1.

6.7 Embedded Operations Channel (eoc) Tests

Protocol testing of the *eoc* exploits the *eoc* protocol feature that the protocol operates in a request/reply manner. The network controls all *eoc* communications to the customer SUT.

The testing methodology described here assumes that the network is sending *eoc* messages to the SUT without any bit errors or violations to the protocol. Therefore, the conformance tests described test only the SUT since the operation of the protocol from the network side is always correct. With the network sending a variety of *eoc* messages in a controlled sequence, the SUT can be tested for protocol conformance based on the actions the SUT takes. The actions taken by the SUT can then be compared to the known correct responses.

Under the testing methodology described above, the SUT can be tested for conformance in the following two ways:

- Function Activation Testing

  The SUT should activate the correct function corresponding to the *eoc* message frame received when receiving the frame three times identically, consecutively, and with the proper addressing.

- Interface Conformance Testing

  The SUT should send back to the network an appropriate response *eoc* frame for each *eoc* frame received from the network. The *eoc* response frame sent by the SUT to the network depends on the information contained in all of the bits (12 bits) comprising the *eoc* frame that the SUT originally received.

The above two testing criteria form the basis for designing *eoc* test scripts for testing the SUT.

There are three test scripts documented here that provide tests for determining if the *eoc* processing in the SUT is in conformance with ANS T1.601-1988, section 8.3. When observing the three test scripts collectively, the SUT is to receive every 12-bit combination possible as input *eoc* frames. This method, therefore, checks conformance with 100% confidence. In addition, the actions and *eoc* responses taken by the SUT for each *eoc* input frame will be compared to the correct SUT actions and *eoc* responses.

See figures 16 and 17 below for diagrams summarizing the operation of the *eoc* protocol as defined in ANS T1.601-1988.

EQUIPMENT:
• Layer 1 tester capable of sending various *eoc* messages and capturing the corresponding received *eoc* frame outputs of the SUT

CONFIGURATION:
See figure 15.

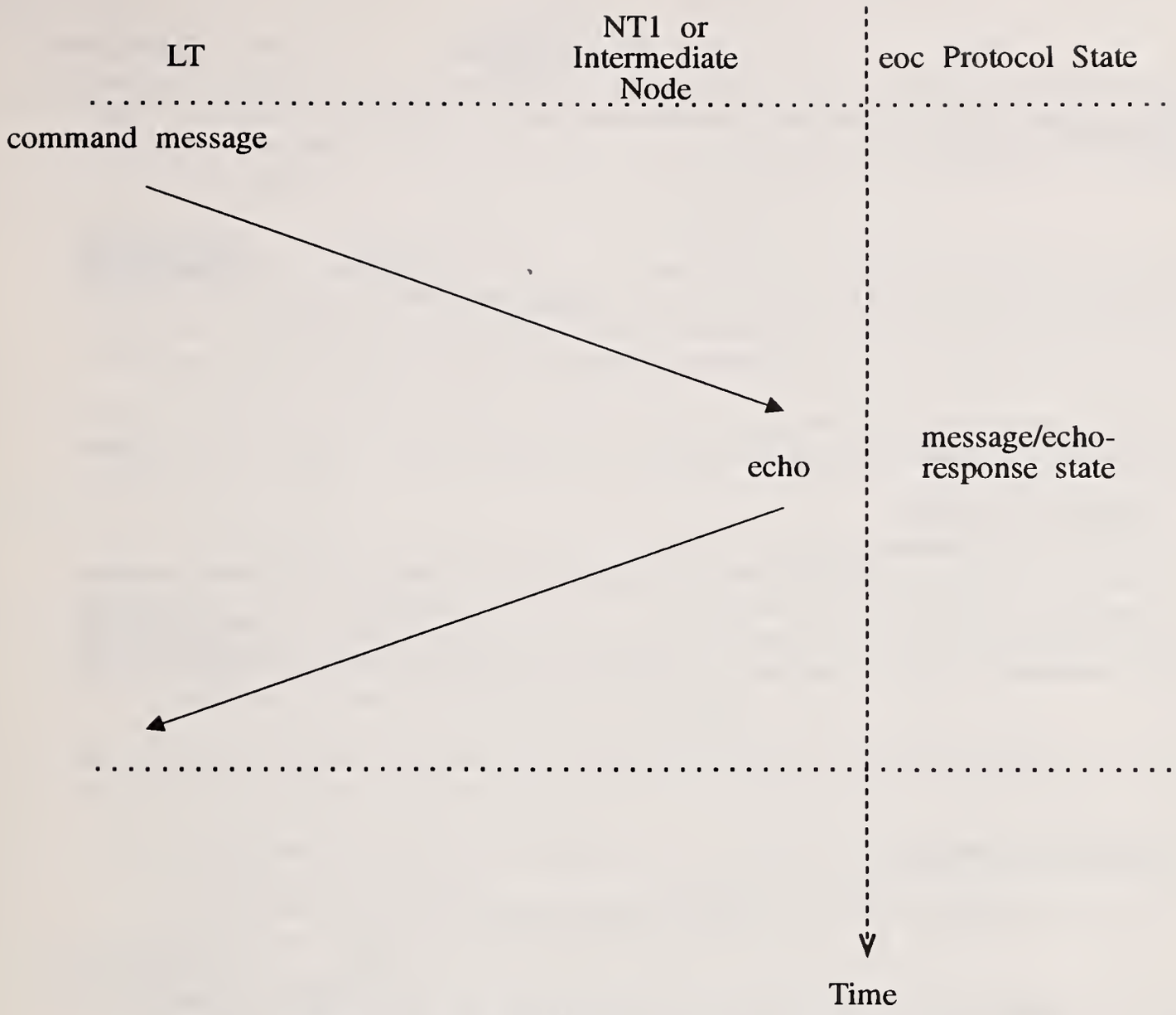


Figure 16. Command/Response eoc Protocol Mode.

For an error free *eoc*, the Command/Response mode is completed with three cycles of the message/echo response state.

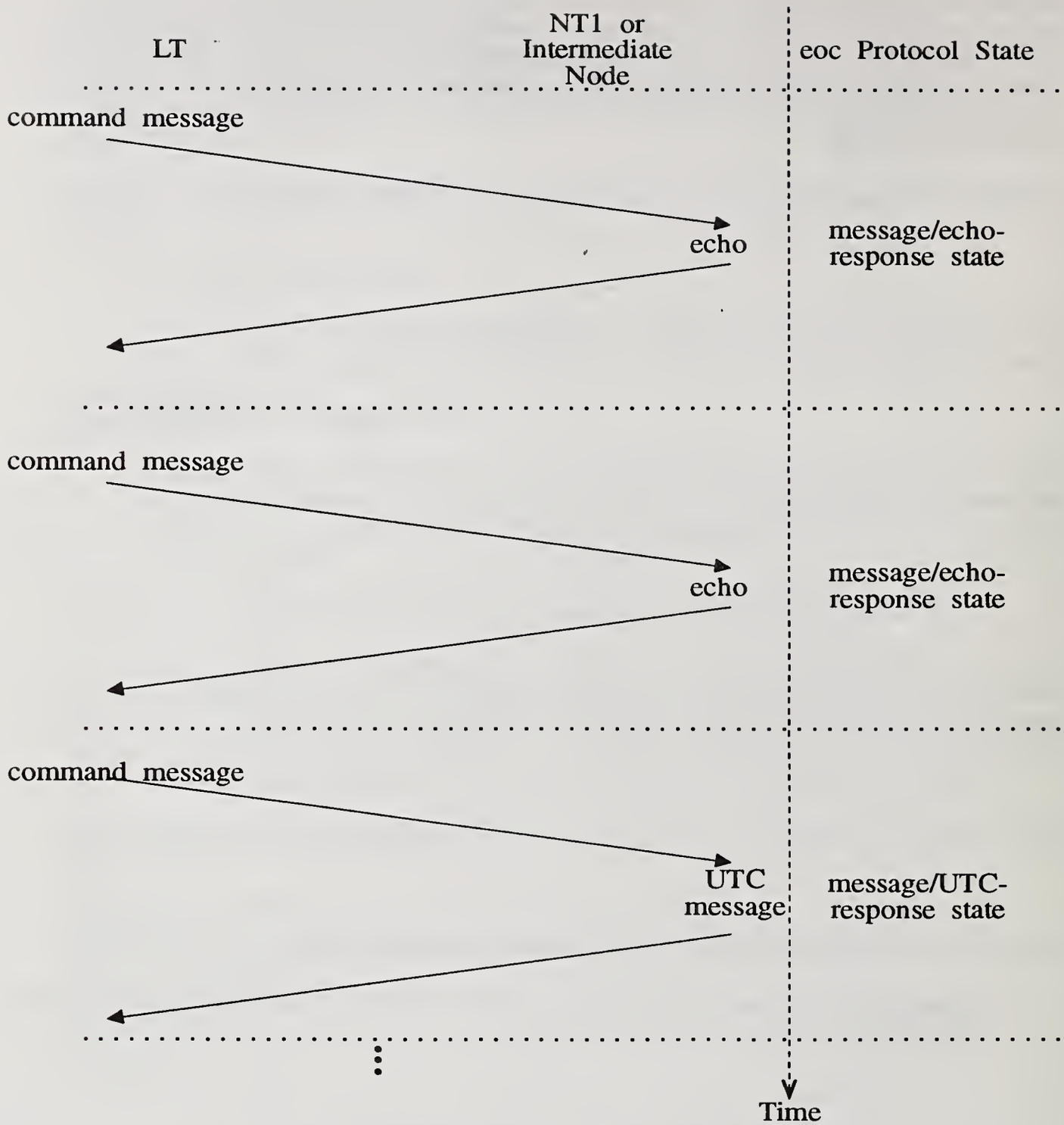


Figure 17. Unable-to-Comply (UTC) eoc Protocol Mode.

For an error free *eoc*, the message/UTC-response state is always preceded by two cycles of the message/echo-response state. The UTC mode concludes on an error free *eoc* with three cycles of the message/UTC-response state. With errors present on the *eoc*, the message/UTC-response state will be repeated until three identical and consecutive UTC response messages are received by the LT.

6.7.1 Test Script #1

PURPOSE:
Test Script #1 tests the SUT actions and *eoc* responses when the network is sending it *eoc* frames at least three times, identically and consecutively that should not result in any operations function being activated at the SUT. During this test script, the corresponding *eoc* response frames from the SUT vary depending on the specific input frame.

PROCEDURE:
In Test Script #1, each unique frame transmitted by the network is sent enough times consecutively for the SUT to activate an operations function if instructed. However, only *eoc* frames that should **not** result in any operation function becoming latched at the SUT are sent during Test Script #1. Therefore, the focus of Test Script #1 is to observe the *eoc* frame responses from the SUT.

Before Test Script #1 is started, the SUT should not have any operations functions latched. In addition, throughout the Test Script #1 sequence, the SUT should be constantly observed to verify that no operations functions become latched.

There are a total number of 4096 (2 to the power of 12) possible 12-bit *eoc* frame encodings. Out of these encodings, there are a total of 4086 unique *eoc* frames that can be sent by the network (with encodings in the range from "0000 0000 0000" to "1111 1111 1111") that **will not** cause the SUT to activate any operations function. In Test Script #1, each of the 4086 encodings (*eoc* frames) is transmitted by the network to the SUT five times identically and consecutively. In addition, to simplify test implementation, the *eoc* frames that are transmitted are sent in numerical order.

The *eoc* frames sent by the network in Test Script #1 and the subsequent responses from the SUT are listed below in the order followed by the test script:

1. Input Frames: The frames are addressed to the SUT and contain all data byte values. (number of unique input frames = 256)
(Address Field = 000, Data/Message Indicator = 0, Information Field = 00000000 to 11111111)
(total number of input frames transmitted by network = 5 x 256 = 1280)

   Output Frames: For each unique input frame sent five times, the response should be two echo frames plus three frames containing the SUT address and the Unable to Comply message.

   Note: The requirement for an "Unable-to-Comply" response to a data byte addressed to an NT that does not support a data reception feature is not made specifically clear in ANS T1.601-1988 but is expected to be a part of the ANS T1.601-1991 (revised standard). Implementations of *eoc* capabilities existing on the date of publication of the 1991 edition or which are new within a period of one year thereafter will be exempt from this requirement.

2. Input Frame: The frame is addressed to the SUT and contains the Hold State message
(total number of unique input frames = 1)
(Address Field = 000, Data/Message Indicator = 1, Information Field = 00000000)
(total number of input frames transmitted by network = 5)

   Output Frames: The response should be five echo response frames.

3. Input Frames: The frames are addressed to the SUT and contain all unknown messages.

(number of unique input frames = 249)
(Address Field = 000, Data/Message Indicator = 1, Information Field = 00000001 to 01001111)
(Address Field = 000, Data/Message Indicator = 1, Information Field = 01010101 to 11111110)
(total number of input frames transmitted by network = 5 x 249 = 1245)

Output Frames: For each unique input frame sent five times, the response should be two echo frames plus three frames containing the SUT address and the Unable to Comply message.

4. Input Frame: The frame is addressed to the SUT and contains the Return to Normal Message.
(number of unique input frames = 1)
(Address Field = 000, Data/Message Indicator = 1, Information Field = 11111111)
(total number of input frames transmitted by network = 5)

Output Frames: The response should be five echo response frames.

5. Input Frames: The frames have non-SUT and non-broadcast addresses and contain any message or data byte value.
(number of unique input frames = 3072)
(Address Field = 001 to 110, Data/Message Indicator = 1 and 0, Information Field = 00000000 to 11111111)
(total number of input frames transmitted by network = 5 x 3072 = 15,360)

Output Frames: For each unique input frame sent five times, the response should be five frames containing the SUT address and the Hold State message.

6. Input Frames: The frames have the broadcast address and contain all data byte values.
(number of unique input frames = 256)
(Address Field = 111, Data/Message Indicator = 0, Information Field = 00000000 to 11111111)
(total number of input frames transmitted by network = 5 x 256 = 1280)

Output Frames: For each unique input frame sent five times, the response should be two echo frames plus three frames containing the SUT address and the Unable to Comply message.

7. Input Frame: The frame has the broadcast address and contains the Hold State message.
(number of unique input frames = 1)
(Address Field = 111, Data/Message Indicator = 1, Information Field = 00000000)
(total number of input frames transmitted by network = 5)

Output Frames: The response should be five echo response frames.

8. Input Frames: The frames have the broadcast address and contain all unknown messages.
(number of unique input frames = 249)
(Address Field = 111, Data/Message Indicator = 1, Information Field = 00000001 to 01001111)
(Address Field = 111, Data/Message Indicator = 1, Information Field = 01010101 to 11111110)
(total number of input frames transmitted by network = 5 x 249 = 1245)

Output Frames: For each unique input frame sent five times, the response should be two echo frames plus three frames containing the SUT address and the Unable to Comply message.

9. Input Frame: The frame has the broadcast address and contains the Return to Normal Message.

(number of unique input frames = 1)

(Address Field = 111, Data/Message Indicator = 1, Information Field = 11111111)
(total number of input frames transmitted by network = 5)

Output Frames: The response should be five echo response frames.

PASS-FAIL CRITERIA:
Observing transmitted and corresponding received *eoc* frames as exactly specified in Test Script #1 shall constitute passing Test Script #1. Any observed variation from Test Script #1 shall constitute failure of Test Script #1.

6.7.2 Test Script #2

PURPOSE:
The *eoc* frames sent to the SUT in Test Script #2 contain known messages with proper addressing but are not sent three times identically and consecutively. Therefore, in Test Script #2 the SUT should also not activate any operations functions.

Test Script #2 tests the *eoc* protocol rule that a properly addressed and known message should activate the corresponding operations function in the SUT only if the *eoc* frame is received by the SUT three times identically and consecutively.

PROCEDURE:
In Test Script #2, the input frames are addressed correctly for the SUT (i.e., SUT address or broadcast address) and contain known messages, however, they are **not** sent 3 times identically and consecutively. Therefore, no operations functions should be latched at the SUT as a result of any *eoc* messages sent during Test Script #2.

In Test Script #2, each of the seven *eoc* messages known by the SUT is transmitted by the network with correct addressing to the SUT two times identically and consecutively. Every third consecutive message sent is the Hold State message (with correct addressing). This pattern of input messages to the SUT should **not** be sufficient to cause the SUT to activate the known message since any known message is never received by the SUT three times identically and consecutively.

Another way that Test Script #2 transmits properly addressed and known *eoc* messages to the SUT without causing any operations function to become latched is to send each known message only one time identically and consecutively. That is, every second and third consecutive *eoc* message is the Hold State message. In this scenario, the pattern of input messages to the SUT again should **not** be sufficient to cause the SUT to activate the known message since any known message is never received by the SUT three times identically and consecutively.

The total number of *eoc* input frames transmitted by the network in Test Script #2 equals 84 frames. All response *eoc* frames from the SUT in Test Script #2 should be echo frames.

PASS FAIL CRITERIA:
Observing transmitted and corresponding received *eoc* frames as exactly specified in Test Script #2 shall constitute passing Test Script #2. Any observed variation from Test Script #2 shall constitute failure of Test Script #2.

6.7.3 Test Script #3

PURPOSE:
In Test Script #3, known messages with proper addressing are sent to the SUT three times identically and consecutively. The messages sent to the SUT are in a special sequence to properly test that the SUT is activating the correct operations functions at the proper time.

Up until this point, if the SUT is functioning properly, neither *eoc* frames sent in Test Script #1 nor Test Script #2 should result in the SUT latching an operation function. Consequently, Test Script #3 provides tests to determine if the SUT will latch the correct operations function upon receiving three identical, consecutive, and properly addressed *eoc* frames containing a known message.

PROCEDURE:
The *eoc* frame encodings corresponding to known messages that are sent in Test Script #3 are not in numerical order as in the previous test scripts. However, the order in which they are sent allows all known messages to be tested with respect to each other. For example, after each Return to Normal message is received by the SUT correctly (i.e., with proper address and three times identically and consecutively) any operations functions previously activated are unlatched. Also, in Test Script #3, the Hold State message is always received by the SUT correctly after a new operations function has just been previously latched. Therefore, the SUT should continue to maintain all latched operations functions upon receiving the Hold State message correctly.

In Test Script #3, the seven known messages are each transmitted by the network three times consecutively. However, the Hold State and the Return to Normal messages are sent three times consecutively many times within the message sequence which results in a total of 84 *eoc* frames being transmitted by the network.

Each *eoc* frame transmitted by the network is sent out three times consecutively. Because the *eoc* frames received by the SUT contain known messages that are properly addressed, all SUT response frames in Test Script #3 are echo *eoc* frames.

The *eoc* frames sent by the network in Test Script #3 and the subsequent responses from the SUT are listed below in the order followed by the test script:

1. Input Frames: Return to Normal message (eoc Frame = 000111111111)

   Output Frames: echo frames

   The SUT after receiving the input frames should have all operations function unlatched.

2. Input Frames: Operate 2B+D Loopback message (eoc Frame = 000101010000)

   Output Frames: echo frames

   The SUT after receiving the input frames should latch the 2B+D loopback

3. Input Frames: Hold State message (eoc Frame = 000100000000)

   Output Frames: echo frames

   The SUT after receiving the input frames should still have the pending 2B+D loopback latched.

4. Input Frames: Return to Normal message (eoc Frame = 000111111111)

   Output Frames: echo frames

   The SUT after receiving the input frames should have all operations function unlatched.

5. Input Frames: Operate B1 Loopback message (eoc Frame = 000101010001)

   Output Frames: echo frames

   The SUT after receiving the input frames should latch the B1 loopback.

6. Input Frames: Hold State message (eoc Frame = 000100000000)

   Output Frames: echo frames

   The SUT after receiving the input frames should still have the previous B1 loopback latched.

7. Input Frames: Operate B2 Loopback message (eoc Frame = 000101010010)

   Output Frames: echo frames

   The SUT after receiving the input frames should latch the B2 loopback.

8. Input Frames: Hold State message (eoc Frame = 000100000000)

   Output Frames: echo frames

   The SUT after receiving the input frames should still have the previous B2 loopback latched.

9. Input Frames: Return to Normal message (eoc Frame = 000111111111)

   Output Frames: echo frames

   The SUT after receiving the input frames should have all operations function unlatched.

10. Input Frames: Request Corrupted crc message (eoc Frame = 000101010011)

    Output Frames: echo frames

    The SUT after receiving the input frames should start sending corrupted crcs.

11. Input Frames: Hold State message (eoc Frame = 000100000000)

    Output Frames: echo frames

    The SUT after receiving the input frames should still be sending corrupted crcs.

12. Input Frames: Notify Corrupted crc message (eoc Frame = 000101010100)

Output Frames: echo frames

The SUT after receiving the input frames should be in the notified state concerning the corrupted crcs.

13. Input Frames: Hold State message (eoc Frame = 000100000000)

Output Frames: echo frames

The SUT after receiving the input frames should have notification of receiving corrupted crcs.

14. Input Frames: Return to Normal message (eoc Frame = 000111111111)

Output Frames: echo frames

The SUT after receiving the input frames should have all operations function unlatched.

15. Input Frames: Return to Normal message (eoc Frame = 111111111111)

Output Frames: echo frames

The SUT after receiving the input frames should have all operations function unlatched.

16. Input Frames: Operate 2B+D Loopback message (eoc Frame = 111101010000)

Output Frames: echo frames

The SUT after receiving the input frames should latch the 2B+D loopback

17. Input Frames: Hold State message (eoc Frame = 111100000000)

Output Frames: echo frames

The SUT after receiving the input frames should still have the pending 2B+D loopback latched.

18. Input Frames: Return to Normal message (eoc Frame = 111111111111)

Output Frames: echo frames

The SUT after receiving the input frames should have all operations function unlatched.

19. Input Frames: Operate B1 Loopback message (eoc Frame = 111101010001)

Output Frames: echo frames

The SUT after receiving the input frames should latch the B1 loopback.

20. Input Frames: Hold State message (eoc Frame = 111100000000)

Output Frames: echo frames

The SUT after receiving the input frames should still have the previous B1 loopback latched.

21. Input Frames: Operate B2 Loopback message (eoc Frame = 111101010010)

Output Frames: echo frames

The SUT after receiving the input frames should latch the B2 loopback.

22. Input Frames: Hold State message (eoc Frame = 111100000000)

Output Frames: echo frames

The SUT after receiving the input frames should still have the previous B2 loopback latched.

23. Input Frames: Return to Normal message (eoc Frame = 111111111111)

Output Frames: echo frames

The SUT after receiving the input frames should have all operations function unlatched.

24. Input Frames: Request Corrupted crc message (eoc Frame = 111101010011)

Output Frames: echo frames

The SUT after receiving the input frames should start sending corrupted crcs.

25. Input Frames: Hold State message (eoc Frame = 111100000000)

Output Frames: echo frames

The SUT after receiving the input frames should still be sending corrupted crcs.

26. Input Frames: Notify Corrupted crc message (eoc Frame = 111101010100)

Output Frames: echo frames

The SUT after receiving the input frames should be in the notified state concerning the corrupted crcs.

27. Input Frames: Hold State message (eoc Frame = 111100000000)

Output Frames: echo frames

The SUT after receiving the input frames should have notification of receiving corrupted crcs.

28. Input Frames: Return to Normal message (eoc Frame = 111111111111)

Output Frames: echo frames

The SUT after receiving the input frames should have all operations function unlatched.

PASS-FAIL CRITERIA:
Observing transmitted and corresponding received *eoc* frames as exactly specified in Test Script #3 shall constitute passing Test Script #3. Any observed variation from Test Script #3 shall constitute failure of Test Script #3.

APPENDIX A LAYER 1 TESTER FUNCTIONS AND TEST CONFIGURATIONS

A.1 Layer 1 Tester Functional Requirements

This section describes a minimal set of components that are needed for layer one conformance testing. The minimal set of components defines a Layer 1 tester that includes both 2B1Q transmitter and 2B1Q receiver functionalities. The Layer 1 tester described here should be able to emulate LT basic functionalities, to provide different types of impairments, and to perform analysis capabilities so that an appropriate environment for verifying ANS T1.601-1988 requirements of a system under test (SUT) can be produced. These 2B1Q transceivers can be either hardware controlled or software controlled or a combination of both. For example, a 2B1Q transmitter can be implemented using hardware components, and a 2B1Q receiver can be implemented by software. The requirements defined in ANS T1.601-1988 are divided into two primary categories due to the nature of the types of conformance testing needed. Requirements that do not need the Layer 1 tester are grouped into the static test category. Requirements that need the Layer 1 tester are grouped into the dynamic test category. Detailed descriptions of these Layer 1 tester functional requirements can be found in section 3 and appendix B. The appendix is by no means intended to constrain the design, the methodology or procedure for a Layer 1 tester.

A.2 Static Test Configuration

Static tests are defined as tests that are related to the near-end and require no interactions between the near-end and far-end 2B1Q transceivers to complete the tests. That is, these static tests can be performed independent of the Layer 1 tester capability. In practice, the test capabilities required for static testing could be part of the Layer 1 tester. A generic simplified block diagram that can be used to perform a specific static test is depicted in figure A-1. The test network shown in figure A-1 may be as simple as a 135 ohms resistor or a longitudinal balance test bridge. These conformance tests include:

- Return Loss
- Longitudinal Balance
- Longitudinal Output Voltage
- Total Transmit Power
- Power Spectral Density
- Transmit Pulse Shape
- Transmitter Linearity

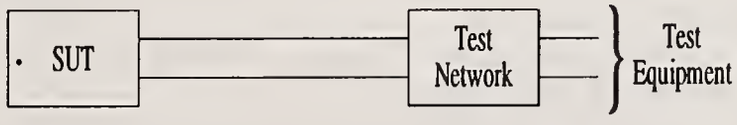


Figure A-1. Simplified Block Diagram for Static Testing.

Except for pulse shape estimation and transmitter linearity, procedures for performing other tests can be found elsewhere in this document. Pulse shape and transmitter linearity measurements can be implemented by software routines. Appendices B and C provide examples and a detailed discussion on a software approach.

A.3 Dynamic Test Configuration

A simplified dynamic test configuration is depicted in figure A-2. The Layer 1 tester block diagram is composed of a 2B1Q transmitter and a 2B1Q receiver. As mentioned above, this Layer 1 tester can be implemented in either hardware, software, or a combination of both. Appendix B provides a detailed discussion of a 2B1Q receiver implementation. The appendix provides examples and is included for reference purposes only; the information in the appendix is by no means intended to constrain the design, the methodology or procedures to perform ISDN conformance testing. Dynamic tests are defined as tests that require interactions between the near-end and the far-end 2B1Q transceivers. These tests include jitter, start-up process, bitstream generation/verification, and M-channel generation/verification. Figure A-2 can be used generically to perform these tests.

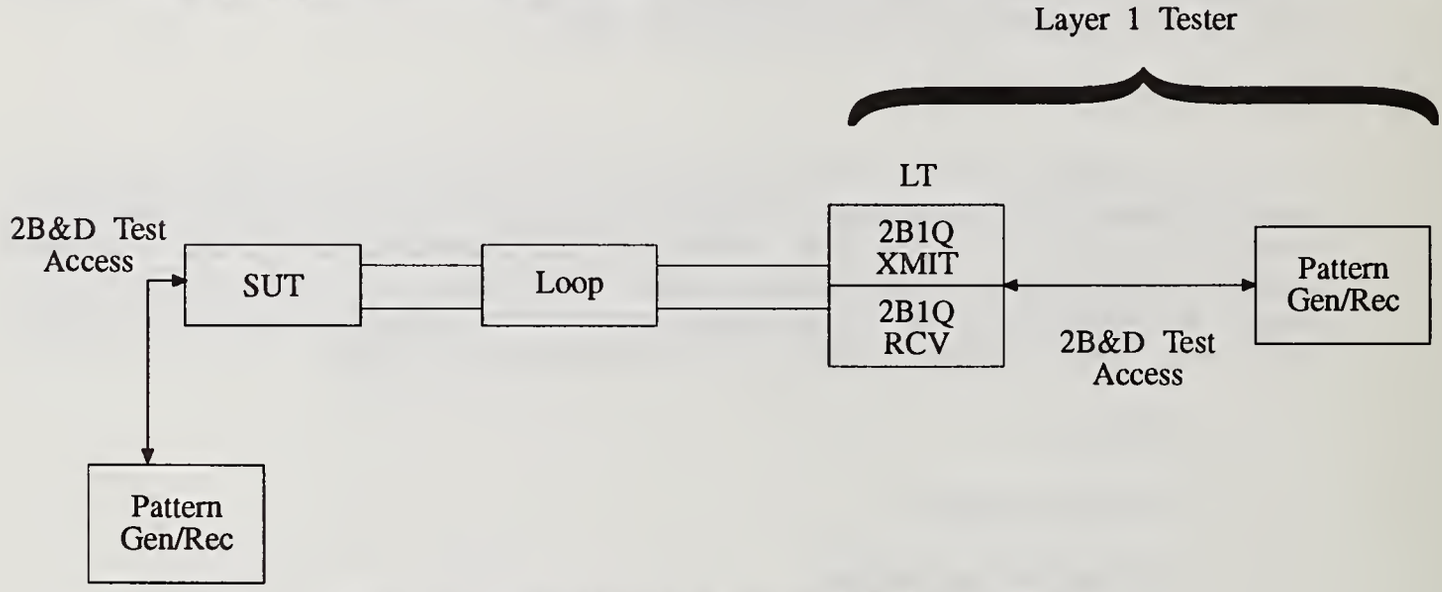


Figure A-2. Simplified Block Diagram for Dynamic Testing.

A.3.1 Layer 1 Test Transmitter Requirements

A 2B1Q transmitter that emulates an LT should be able to perform/provide the following minimal set of functions:

(1) Controllable Transmit Jitter

(2) Transmit Variable Pulse Shapes

(3) Transmitter Linearity

(4) LT 2B1Q Functionalities for the Start-Up Process

(5) Emulating Layer One Tear-Down Conditions

(6) M-Channel Bit Functions

(7) 2B1Q Bitstream Generation

A.3.1.1 Controllable Transmit Jitter

The 2B1Q transmitter that emulates an LT should be able to inject various magnitudes of jitter/wander into a transmitted bitstream as specified in ANS T1.601-1988, section 7.4.1. A variable jitter parameter will allow flexibility in testing different cases where the input signal at the SUT is subject to various amount of jitter. Single jitter frequencies on the LT transmitted signal toward the SUT shall be as specified in ANS T1.601-1988, figure 20.

A.3.1.2 Transmit Variable Pulse Shapes

The output signal of the 2B1Q transmitter that emulates an LT must fall within the pulse mask specified in ANS T1.601-1988, section 5.3.1. It is desirable that the 2B1Q transmitter be able to produce more than one pulse shape. For example, the 2B1Q transmitter may produce different pulse shapes in which one hugs the maximum template, one hugs the minimum template, one falls in between the two templates, or one has a long tail. Because there are other constraints, e.g., total power and power spectral density, the choice of more than one pulse shape would be somewhat more complex. However, this will increase the flexibility of the conformance testing and will also be beneficial to the margin test. The shape of the Layer 1 tester transmitted signal should be randomly selected from a number of available pulse shapes that meet the pulse template, total power, and power spectral density requirements. Examples of two pulse shapes are provided in figures A-3 and A-4. Note that pulse A and pulse B are almost identical except for the tail of pulse B where it oscillates more than pulse A. Both pulses meet the total power and power spectral density constraints as specified in ANS T1.601-1988.

The Layer 1 tester, in addition to transmitting variable pulse shapes, should also have the capability of displaying the basic transmit/received pulse shapes.

A.3.1.3 Transmitter Linearity

The residual rms signal (nonlinearity) at the transmitter output of the Layer 1 tester as specified in ANS T1.601-1988, section 5.3.3 and appendix D, must be at least 36 dB below a perfectly linear signal. Since this requirement applies to all normal transceivers under test, it is desirable that the SUT be subject to different nonlinearity ratios. That is, the Layer 1 tester should be able to produce signals with residual rms signal of 36 dB (worst case condition).

A.3.1.4 LT 2B1Q Functionalities for the Start-up Process

The Layer 1 tester transmitter should be able to provide the following basic LT functionalities for testing the SUT start-up process:

- Generating the LT activation signals (TL, SL1, SL2, and SL3)
- The LT line rate during start-up must be 80 kbaud ±5 ppm.
- A variable start-up sequence is desirable in order to verify that the SUT sends activation signals (TN, SN1, SN2, SN3) at the correct instant. A minimum of two start-up sequences should be used. The first sequence should omit the SL1 signal since this signal is considered optional by the standard.

- Initiating start-up from the Layer 1 tester while the SUT is in the RESET state.

- Responding appropriately to start-up from customer equipment (ANS T1.601-1988, sec. 6.4.6.2).

- Simulating LT behavior (warm start or cold start) to test a warm-start NT1 SUT.

A.3.1.5 Emulating Layer 1 Tear-Down Conditions

The Layer 1 tester should be able to generate corrupted SW/ISW in order to verify the SUT's ability to enter/exit the tear-down correctly. It is suggested that all 9 symbols of the SW/ISW be corrupted to enforce a tear-down. The purpose of generating the corrupted SW/ISW is to simulate the cold start failure and loss of synchronization conditions.

The Layer 1 tester must have the ability to stop transmitting signal to the SUT for at least 480 ms to produce the loss of signal condition, and thus enforce a tear-down at the SUT. Also, it is desirable that the Layer 1 tester can stop sending signal for less than 480 ms interval so that the SUT's behaviors can be monitored.

A.3.1.6 M-Channel Bit Functions

The Layer 1 tester must be capable of generating/performing the following M-Channel bit functions:

(1) Generate corrupted crc bits for single superframes or for any pre-defined time interval.

(2) Generate eoc messages to support operations communications between the Layer 1 tester and the SUT. These eoc messages should include: unable-to-comply acknowledgment, request corrupt crc, notify of corrupted crc, and hold state.

A.3.1.7 2B1Q Bitstream Generation

The Layer 1 tester must be able to pair, scramble, code and frame the binary bitstream. The Layer 1 tester must transmit 2B1Q bitstreams as defined in ANS T1.601-1988 including the control of B_1, B_2, and D channel transmit data.

A.3.1.8 Sealing Current Generation

The Layer 1 tester should provide sealing current as defined in ANS T1.601-1988, section 7.5.1.

A.3.2 Layer 1 Test Receiver Requirements

A 2B1Q receiver must be able to perform the following minimal set of functions:

(1) Receive Jitter Measurement

(2) Start-Up Process Verification

(3) Bitstream/Baud Rate Verification

A.3.2.1 Receive Jitter Measurement

The 2B1Q receiver should be able to capture signals originated from the SUT so that the SUT's output signal jitter can be verified as specified in ANS T1.601-1988, section 7.4.2. The tolerance of the SUT to jitter from the Layer 1 tester is verified by the performance tests outlined elsewhere. The measurement can be implemented by the use of either test equipment or software routine. An example of an off-line jitter calculation algorithm used to compute adherence to the requirements is provided in appendix C.

A.3.2.2 Start-Up Process Verification

The receiver of the Layer 1 tester must be capable of detecting activation signals from the SUT such as TN, SN1, SN2, and SN3 and providing time stamps upon detection of each signal during the start-up process under various circumstances as specified in ANS T1.601-1988 (e.g., loss of signal, loss of synchronization, failure to start-up). Further discussions and examples of test configurations can be found in section 5 of this document.

A.3.2.3 Bitstream Verification

In order to verify the SUT's output signal,the 2B1Q receiver must be able to decode, descramble, and deframe the received signals. The TN, SN1, SN2, and SN3 signals from the SUT must be captured by the 2B1Q receiver to verify that they conform to the ANSI signal definition. In addition, the 2B1Q receiver must provide a B_1, B_2, and D channel pattern search capability.

The 2B1Q receiver must also verify the baud rate of the free-running SUT. Alternatively, this baud rate test can also be included under the static test category.

A.3.2.4 eoc Message Detection

The 2B1Q receiver must be able to detect return eoc messages originated from the SUT as defined in ANS T1.601-1988, section 8.3.

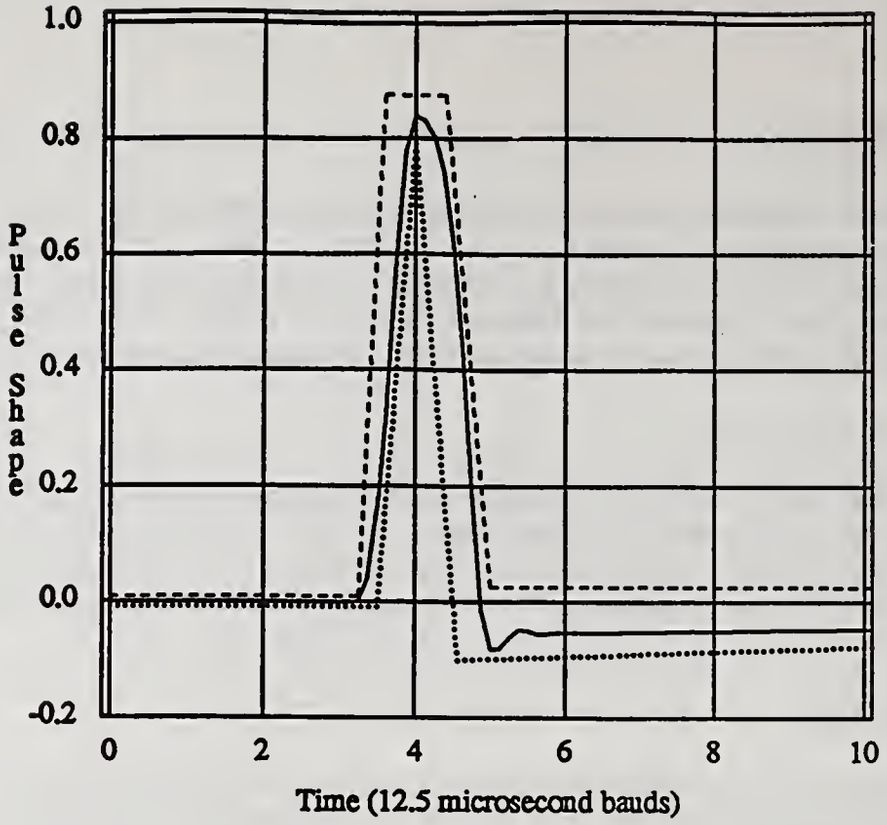


Figure A-3. Layer 1 Transmitter Pulse Shape A.

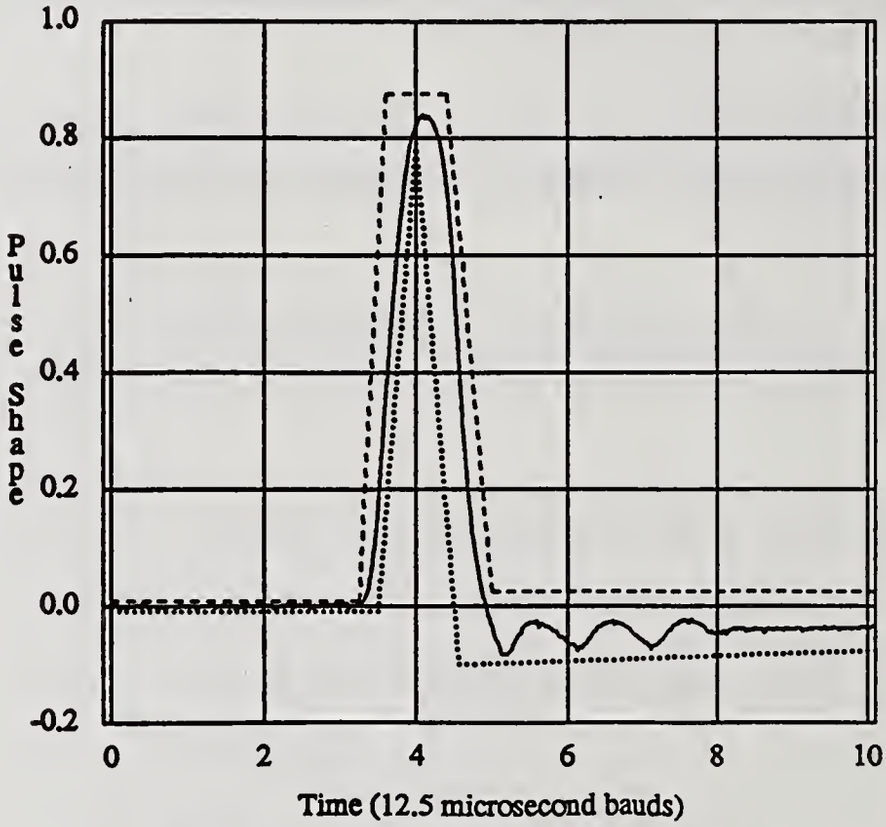


Figure A-4. Layer 1 Transmitter Pulse Shape B.

APPENDIX B LAYER 1 TESTER RECEIVER

B.1 Receive Pulse Shape

The 2B1Q receiver should be able to capture signals originated from the SUT so that its pulse shape compliance can be verified. Under normal operation, it is impossible to transmit an isolated pulse onto the line because of the 2B1Q property. Each baud interval of a 2B1Q line code contains energy from not just one pulse but from adjacent pulses. Furthermore, changing the pulse pattern does not alleviate the difficulty of detecting an isolated pulse because there are no "null" pulses. Therefore, it is very complex to measure an isolated pulse. However, the pulse shape can be verified by processing the captured data using software routines. For illustration purposes, this section discusses a methodology of implementing such routines.

The only basic hardware components that are needed to capture the SUT's transmitted 2B1Q signal are a real time waveform digitizer to capture samples of the SUT's output signal and a digital computer to process the captured signal. The waveform recorder must have an accuracy of at least 12 bits to satisfy the ANSI's requirement of 12 bits resolution on linearity tests. It might be necessary to pre-process the captured waveform prior to running the pulse shape estimation routines. If the SUT's output signal includes other unwanted components, the captured waveform must be pre-processed to remove the unwanted energy. However, to simplify the post-processing software, the SUT's output signal is captured as it transmits into a 135 ohm load. That is, the captured signal does not contain the far end signal. The captured waveform becomes input data for the pulse shape estimation software.

The software approach uses adaptive signal processing to estimate the basic transmitted pulse shape. The Kalman algorithm [HAYD86] was chosen in favor of the least mean square (LMS) algorithm and Wiener filtering since each Kalman filter's updated estimate can be computed from previous estimate and the new input data. Therefore, only the previous estimate must be stored. Furthermore, in addition to eliminating the need for storing the entire past observed data, the Kalman algorithm is computationally more efficient than computing the estimates directly from the entire past observed data at each step.

Four assumptions were made in calculating the pulse shape. First, it is assumed that the SUT's pulse shape for each of the four possible quaternary symbols is a scaled version of the pulse for the +1 symbol. The second assumption is that the symbols have the perfect ratio 3:1:-1:-3. Under this linearity assumption, the SUT's output signal can be expressed as the convolution of the transmitted symbols with the unknown SUT's pulse shape. Thus, pulse shape evaluation can be expressed in terms of the system identification problem (i.e., given the input signal, find the system impulse response that results in the known corresponding output signal). The third assumption is that the transmitted symbols (input signal) is known before the system identification process. Two approaches can be considered in determining the input symbols: 1) constrain the coder input to a known pattern (e.g., sync word), or 2) apply a receiver routine to determine the imbedded symbols directly. The fourth assumption deals with the unknown system delay. This delay must be determined before the application of the pulse shape estimation.

With the above assumptions, what follows is a general discussion of the application of adaptive Finite Impulse Response (FIR) digital filtering to pulse shape estimation.

Figure B-1 is a block diagram that demonstrates the use of an adaptive filter in estimating the impulse response of an unknown system (i.e., basic transmitter pulse shape). An adaptive FIR filter is one whose tap weights are subject to continuous modification by an adaptive control algorithm. The tap update algorithm is driven by the difference between the adaptive filter output $\hat{y}(n)$ and the "desired" response $y(n)$

in an attempt to minimize some measure of this difference. If $u(n)$ and $y(n)$ are the input and output signals, respectively, then the unknown system can be described as:

$$y(n) = \sum_{k=-\infty}^{\infty} u(k)h(n-k), \qquad n \geq 0.$$

The unknown system impulse response, $h(n)$, is related to the basic transmitter pulse shape by the relation:

$$h(n) = p(n-\tau)$$

where $p(n)$ is the basic transmitter pulse shape, and τ is the delay between the input and output signals.

The input sequence $u(n)$ is applied to the adaptive filter with tap weights $w_1^*(n)$ through $w_M^*(n)$ which results in the estimated output $\hat{y}(n)$.

$$\hat{y}(n) = w^H(n)u(n)$$

where H denotes Hermitian transposition of the M-by-1 tap weight vector $w(n)$, and $u(n)$ is the M-by-1 input vector. The objective of the update algorithm is to minimize the mean square value of the error $e(n)$ between the desired response, $y(n)$, and the estimated response, $\hat{y}(n)$. The estimation error can be expressed as: .

$$e(n) = y(n) - \hat{y}(n).$$

The objective is to minimize the mean square error, $J(w)$:

$$J(w) = E[e(n)e^*(n)]$$

so that the estimate of the tap weight vector, $w(n)$, produced by the Kalman algorithm approaches the optimum Wiener solution, $w_o(n)$. This optimum Wiener solution, $w_o(n)$, is the estimated basic transmitter pulse shape.

A brief review of the Kalman algorithm is provided below. An in-depth discussion of this subject is given in reference [HAYD86]. The process equation for the Kalman filter is:

$$w_o^*(n+1) = w_o^*(n)$$

and the measurement equation is:

$$y(n) = u^T(n)w_o^*(n) + e_o(n)$$

where $e_o(n)$ is the optimum estimation error left by the Wiener filter. A summary of Kalman algorithm for adaptive transversal filters is given in table B-1.

B.2 Transmitter Linearity

The residual rms signal at the transmitter output of the SUT must be at least 36 dB below a perfectly linear signal as specified in ANS T1.601-1988, section 5.3.3. The 2B1Q receiver should be able to capture the SUT output signal to check for linearity. This linearity test can be implemented by processing the captured signal using software routines.

Similar to the pulse shape compliance test, the transmitter linearity is performed using the same system configuration as that of the pulse shape estimation. The system identification model of pulse shape estimation developed above can also be used to measure transmitter nonlinearity. The system identification developed in previous section can be modified to include a nonlinearity term:

$$y(n) = \eta(n) + \sum_{k=-\infty}^{\infty} u(k)h(n-k), \qquad n \geq 0.$$

Figure B-2 is a block diagram that demonstrates the use of an FIR filter in estimating the impulse response of an unknown system. Ideally, the linear portion of the transmitter output is removed from the signal, leaving only the residual nonlinear component behind. This is accomplished by applying the imbedded symbol sequence to a linear filter which is matched in a mean square sense to the transmitter transfer function and subtracting the filter output from the transmitter output. In actuality, the linear portion of the signal beyond the time range of the FIR filter will also remain, although its contribution can be made negligibly small, $e_o(n)$. The transmitter nonlinearity is modeled as a zero mean random process added to the linear portion of the transmitter output. The transmitter nonlinearity (mean square error) is the difference between the transmitter output and Wiener output as the number of adaptive taps approaches ∞. The goal here is to ensure that the minimum mean square error due to FIR modeling of the IIR is small compared to the portion due to transmitter nonlinearity. Since the nonlinearity is unknown and may be arbitrarily small, it is impossible to guarantee this condition. Instead, we will be content if our goal holds for nonlinearity values near the specified -36 dB relative to total transmitter power. We can then use the measured mean square error as an accurate measure of the transmitter nonlinearity.

REFERENCES:

[HAYD86] S. Haykin, Adaptive Filter Theory, Prentice-Hall, Englewood Cliffs, NJ 1986.

Table B.1.1. Summary of Kalman Algorithm for Adaptive Transversal Filters

Input Variables:

Observed Signal:

$$u(1),u(2),....,u(n)$$

Desired response:

$$y(1),y(2),...,y(n)$$

For n = 1,2,.... compute:

$$g(n) = K(n-1)u(n)[u^H(n)K(n-1)u(n) + J_{min}]^{-1}$$
$$\xi(n) = y(n) - \hat{w}^H(n-1)u(n)$$
$$\hat{w}(n) = \hat{w}(n-1) + g(n)\xi^*(n)$$
$$K(n) = K(n-1) - g(n)u^H(n)K(n-1)$$

Initial conditions:

$$\hat{w}(0) = 0$$
$$K(0) = cI, \qquad c>0$$

Assumption:

J_{min} can be set between 10^{-2} and 10^{-3} times the variance of y(n).

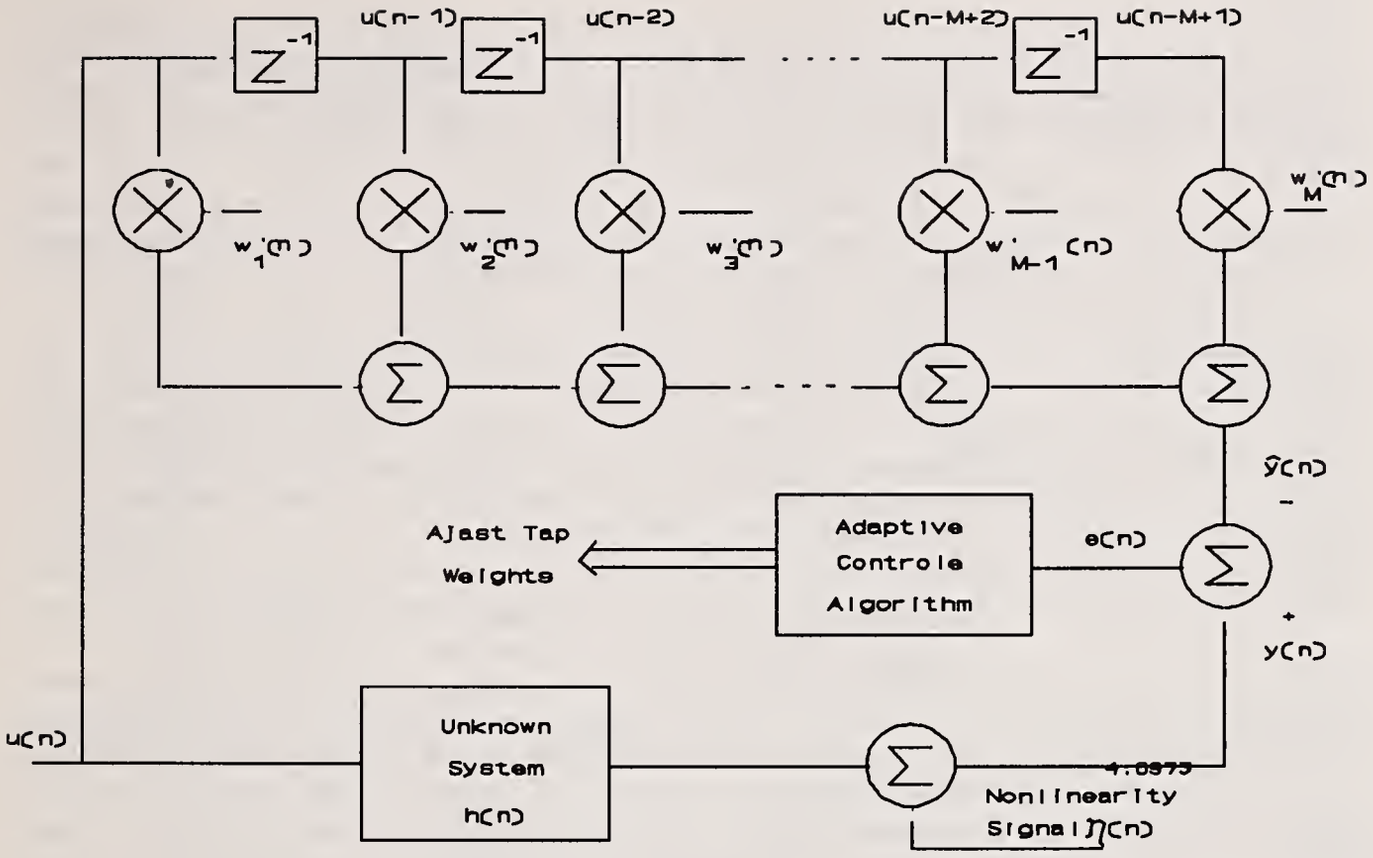


Figure B-1. Impulse Response Estimation Using Adaptive Filter.

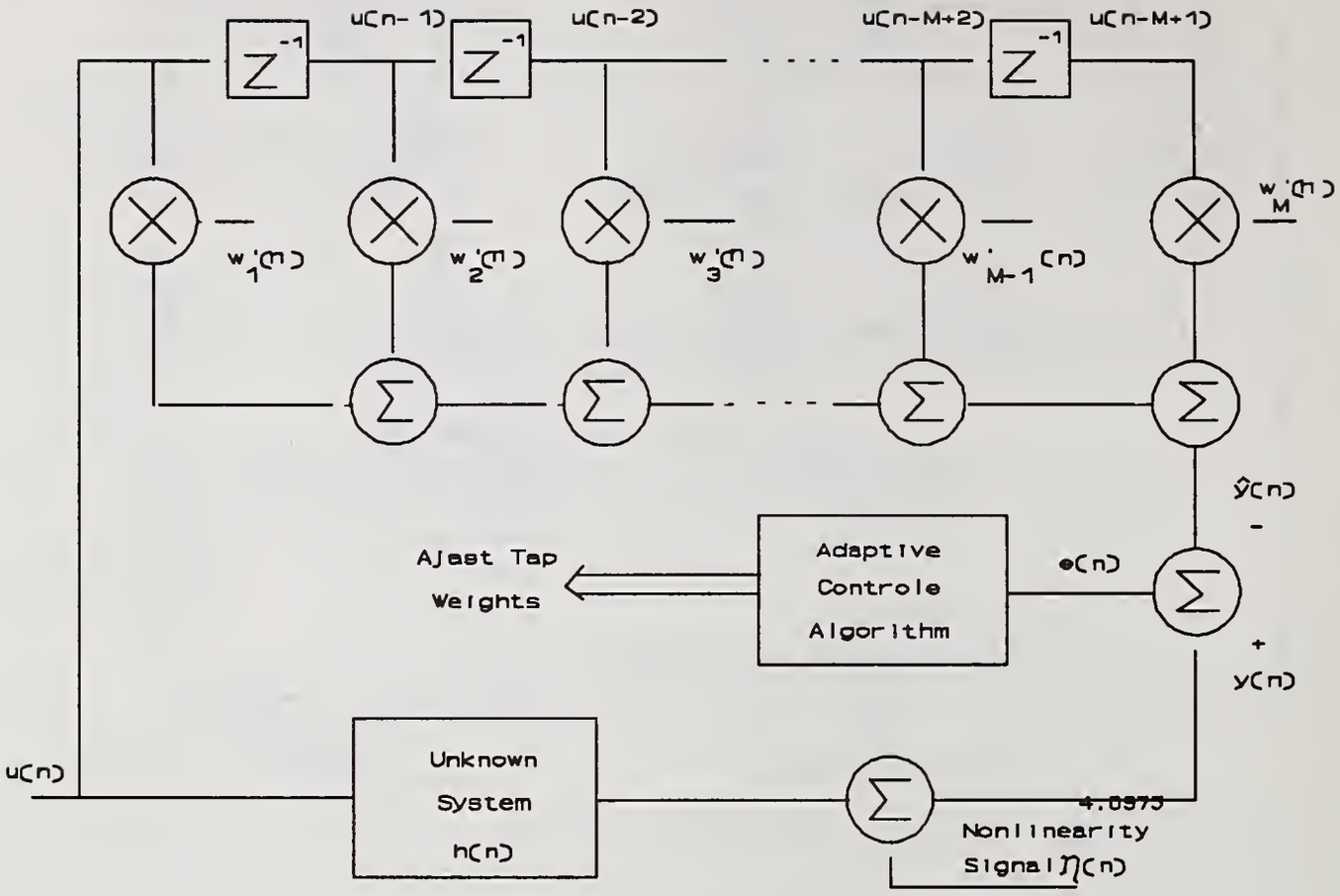


Figure B-2. System Identification with Nonlinearity.

APPENDIX C JITTER ANALYSIS SOFTWARE

The 2B1Q receiver should be able to measure the amount of SUT signal jitter so that compliance to ANS T1.601-1988, section 7.4.2, can be verified. Under normal operation, this is difficult to do for several reasons. First, the 2B1Q signal does not have baud spaced threshold crossings which are normally utilized in timing recovery and jitter analysis algorithms. Second, the SUT continously recovers signal timing from the transmitted network 2B1Q signal during full duplex operation. Furthermore, the ANS T1.601-1988 specifies that the network 2B1Q signal must be jittered while measuring SUT jitter. In the absence of access to an internal SUT baud rate clock, software-based processing must be used for jitter analysis of the actual SUT transmitted signal. This appendix discusses a methodology for implementing such routines.

The only basic hardware components that are needed for jitter analysis are a Layer 1 tester that can jitter the LT transmitted signal under specific control, a real time waveform digitizer to capture the SUT's output signal, and a digital computer to process the captured data. The requirements on the waveform recorder are the same as described in appendix B. The SUT is a fully functional SUT with no special modifications other than those described in other portions of this document. The Layer 1 tester initiates start-up on loop #15 with no jitter on the LT transmitted signal. When full duplex transmission occurs, jitter is introduced on the LT signal. When both transceivers are fully transparent in the presence of LT jitter, the LT and SUT transmitted waveforms are captured. These waveforms become the input for the jitter analysis software.

Before the proceeding with jitter analysis, the pulse shape estimation software must be run on unjittered LT and SUT waveforms (see app. B for pulse shape estimation notes). The LT and SUT pulse shapes from unjittered waveform traces are needed during processing of the jittered signal traces prior to performing the jitter analysis itself. Thus the assumptions mentioned in appendix B regarding pulse shape estimation are valid here. In addition, we assume signal phase modulation, $\varepsilon(t)$, in the jittered signal is an unknown, slowly varying time delay. It should be noted that knowledge of the transmitted symbols is not needed. Therefore symbol recovery routines are not applied.

The jitter analysis software utilizes a timing recovery algorithm described in [OERD88]. The technique is similar to analog square timing recovery methods that examine the phase of the baud rate frequency component in a received signal. In a timing-recovery application, this phase information is used to adjust a phase-locked loop and permit a receiver to track a jittered received signal. In this application, this phase information is compared against the phase of an ideal unjittered baud rate clock (derivation of this clock is discussed later). Differences between these two phase measurements is the phase deviation. Further processing of these phase deviation samples extracts jitter time and frequency domain information.

With the above explanation, what follows is a general discussion of digital timing recovery applied to software jitter analysis. A digital timing recovery algorithm operates on samples of the SUT analog waveform recorded by the waveform digitizer. All signals discussed below refer to discrete time waveform traces.

Figure B-1 is a block diagram that demonstrates use of digital timing recovery. The signal y_{SUT} is the SUT waveform after software echo cancellation processing to remove the far-end LT signal. We assume y_{SUT} was sampled at rate N/T, where T = 12.5 μs = 1 symbol period, and $N \geq 4$.

After echo cancellation, y_{SUT} is passed through a filter that maps the SUT pulse shape into a high-pass raised cosine pulse shape. The result is a 2B1Q signal using a high-pass raised cosine pulse shape in place of the original SUT pulse shape. A high-pass raised cosine is preferrable for jitter analysis because: (1) the high pass function reduces low frequency content introduced by the SUT line transformer, (2) the raised cosine pulse width is chosen to have zero crossings at baud spaced (T seconds) intervals and therefore no inter-symbol interference at those sampling points, and (3) mapping an SUT pulse shape into the same

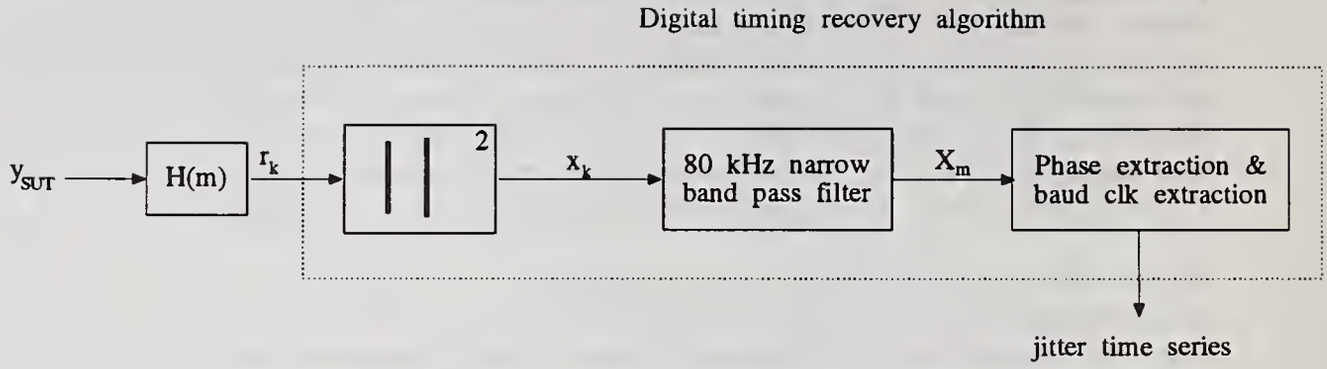


Figure C-1. Use of Digital Timing Recovery in Jitter Analysis.

high-pass raised cosine pulse shape from analysis to analysis reduces jitter measurement variance due to SUT pulse shape dependent parameters. The transfer function of this filter is:

$$H(m) = R_{HP}(m)\frac{R_{RC}(m)}{Y_{SUT}(m)}$$

With:

$R_{HP}(m)$ = single pole high pass filter, f_c=500 Hz.
$R_{RC}(m)$ = discrete fourier transform (DFT) of a raised cosine pulse shape.
$Y_{SUT}(m)$ = DFT of the SUT pulse shape.

It should be noted that the high pass filter pole should be at a sufficiently high frequency to remove low frequency transformer dependent spectral content, but low enough not to adversely affect signal energy. A reasonable criteria is $f_c << 1/2T$.

Squaring the resultant signal places a frequency component at the baud rate 1/T. The new signal can be written as:

$$x_k = \left|\sum_{n=-\infty}^{n=\infty} a_n g\left(\frac{kT}{N} - nT - \epsilon T\right) + \eta\left(\frac{kT}{N}\right)\right|^2$$

With:

g(t) = impulse response of all y_{SUT} pulse shaping filters, including H(m).
$\eta(t)$ = noise components
a_n = transmitted 2B1Q symbols (not needed for jitter analysis)

This represents a signal with a strong frequency component at the baud rate. The spectral component is extracted for every non-overlapping block of length LN samples by computing the complex fourier coefficient:

$$X_m = \sum_{k=mLN}^{(m+1)LN-1} x_k e^{-\frac{j2\pi k}{N}}$$

Here we must balance error performance with the length of LN. We have assumed that $\varepsilon(t)$ varies slowly between successive blocks of LN. Increasing LN reduces error due to $\eta(t)$, but increases error due to assumption violations of $\varepsilon(t)$. Simulation by Oerder and Meyr [OERD88] found that L=64 gives acceptable phase estimation, giving a total length of 256 samples per block for N=4.

The phase estimate $\hat{\varepsilon}_m$ is the phase of this spectral component:

$$\hat{\epsilon}_m = -\frac{1}{2\pi} arg(X_m)$$

Repeating these calculations for the entire waveform trace creates a discrete-time phase estimate $\hat{\varepsilon}_m$ series of $\varepsilon(t)$. From this series, a clock is extracted that "best describes" the SUT system clock in the presence of LT jitter. This becomes the ideal baud rate clock described earlier (this clock must be 80 kHz ±5 ppm). The phase deviation, or jitter, is the difference between $\hat{\varepsilon}_m$ and phase of the ideal "best fit" baud clock. The jitter sequence is the time domain phase deviation series.

This process is repeated on the LT transmitted signal waveform, without echo cancellation, to generate an LT jitter sequence where necessary. Common DFT and time domain analysis techniques are used for further jitter sequence processing specified in ANS T1.601-1988, section 7.4.2.

REFERENCES:

[OERD88] M. Oerder and H. Meyr, "Digital Filter and Square Timing Recovery," IEEE Tranactions on Communications, Vol. 36, May 1988, pp.605 - 611.

APPENDIX D COMPENSATION METHODS FOR LOOP INSERTION LOSS DISCREPANCIES

D.1 Introduction

ANS T1.601-1988 specifies a set of 15 loops that can be used to qualify ISDN transceivers' performance. Although ANS T1.601-1988 provides all 15 loop configurations, it is very difficult to match the cable characteristics of the theoretical models and that of real cables with the specified lengths. This appendix discusses a compensation method for cases where the measured loop insertion loss is higher than the specified/theoretical loop insertion loss. It is very important to consider a compensation method, especially, where an SUT's receiver performance marginally fails the margin requirements specified in T1.601.

D.2 Mean Squared Loss

Mean squared loss (MSL) is a simple method that can be used to compensate for the difference between the theoretical and measured insertion loss values across the frequency band between 0 and 320 kHz. Mean squared loss is defined as:

$$MSL = 10 \log \frac{P_{in}}{P_{out}}$$

P_{in} is the total power, between 0 and 320 kHz, of the transmitted 2B1Q signal used for conformance testing.

P_{out} is the total power, between 0 and 320 khz, of the 2B1Q signal received at the far end. P_{out} is calculated as follows:

$$P_{out} = \int_0^w 10^{\frac{1}{10}[P_1(f)-L(f)]}, \qquad w = 320\ kHz$$

$P_1(f)$ is the power spectral density (PSD) of the transmitted 2B1Q signal used for conformance testing.

$L(f)$ is the measured or calculated loop insertion loss between 0 and 320 kHz.

D.3 Compensation Method

If either the loop simulator or actual cables used for the 15 loops specified in ANS T1.601-1988 have measured loss higher than the theoretical values, compensation for the higher insertion loss must be applied. The following procedure should be used:

- Calculate the insertion loss of the 15 loops specified in ANS T1.601-1988. The insertion loss of the specified loops can be calculated using the primary constants (i.e., resistance (R), inductance (L), conductance (G), and capacitance (C)) provided in ANS T1.601-1988, tables 2 to 4 for PIC (polyethelene insulated cable) cables at 70 °F. Tables D-1 to D-15 of this appendix provide insertion loss values of the specified loops at discrete frequencies based on tables 2 to 4 ANS T1.601-1988, tables 2 to 4.

- Measure the insertion loss of the 15 loops used for conformance testing. Note that these 15 loops must be characterized regardless of whether actual cables or a loop simulator is used.

- Calculate MSL_{meas} based on the measured insertion loss, and MSL_{cal} based on the calculated insertion loss for each loop using the equations above.

· Calculate the difference between MSL_{meas} and MSL_{cal}. This difference is the value that must be used to adjust the 6 dB margin specified in ANS T1.601-1988 for loops 4 to 15. For example, if MSL_{meas} of loop 4 is 2 dB higher than MSL_{cal} based on loop 4 configuration, then the 6 dB margin required in ANS T1.601-1988 is reduced by 2 dB to compensate for the higher insertion loss in the frequency band between 0 and 320 kHz.

Table D.3.1. Insertion Loss Values for Test Loop #1

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	17.91	82.00	56.50	162.00	65.42	242.00	73.17
4.00	21.13	84.00	56.78	164.00	65.61	244.00	73.37
6.00	24.15	86.00	57.05	166.00	65.80	246.00	73.57
8.00	26.79	88.00	57.32	168.00	65.99	248.00	73.77
10.00	29.11	90.00	57.57	170.00	66.18	250.00	73.96
12.00	31.19	92.00	57.82	172.00	66.36	252.00	74.16
14.00	33.06	94.00	58.07	174.00	66.55	254.00	74.36
16.00	34.76	96.00	58.31	176.00	66.74	256.00	74.55
18.00	36.33	98.00	58.54	178.00	66.92	258.00	74.75
20.00	37.76	100.00	58.77	180.00	67.11	260.00	74.94
22.00	39.08	102.00	59.02	182.00	67.29	262.00	75.14
24.00	40.29	104.00	59.27	184.00	67.47	264.00	75.33
26.00	41.42	106.00	59.52	186.00	67.66	266.00	75.53
28.00	42.46	108.00	59.76	188.00	67.84	268.00	75.72
30.00	43.44	110.00	60.00	190.00	68.02	270.00	75.92
32.00	44.34	112.00	60.24	192.00	68.20	272.00	76.11
34.00	45.19	114.00	60.47	194.00	68.38	274.00	76.31
36.00	45.98	116.00	60.70	196.00	68.57	276.00	76.50
38.00	46.73	118.00	60.92	198.00	68.75	278.00	76.70
40.00	47.42	120.00	61.15	200.00	68.93	280.00	76.89
42.00	48.08	122.00	61.37	202.00	69.13	282.00	77.08
44.00	48.70	124.00	61.59	204.00	69.34	284.00	77.28
46.00	49.28	126.00	61.80	206.00	69.54	286.00	77.47
48.00	49.83	128.00	62.02	208.00	69.74	288.00	77.66
50.00	50.35	130.00	62.23	210.00	69.95	290.00	77.86
52.00	50.87	132.00	62.44	212.00	70.15	292.00	78.05
54.00	51.36	134.00	62.65	214.00	70.35	294.00	78.24
56.00	51.83	136.00	62.86	216.00	70.56	296.00	78.44
58.00	52.28	138.00	63.06	218.00	70.76	298.00	78.63
60.00	52.72	140.00	63.26	220.00	70.96	300.00	78.82
62.00	53.13	142.00	63.47	222.00	71.16	302.00	79.02
64.00	53.53	144.00	63.67	224.00	71.36	304.00	79.21
66.00	53.91	146.00	63.87	226.00	71.57	306.00	79.40
68.00	54.27	148.00	64.06	228.00	71.77	308.00	79.60
70.00	54.62	150.00	64.26	230.00	71.97	310.00	79.79
72.00	54.96	152.00	64.46	232.00	72.17	312.00	79.98
74.00	55.29	154.00	64.65	234.00	72.37	314.00	80.17
76.00	55.61	156.00	64.85	236.00	72.57	316.00	80.37
78.00	55.92	158.00	65.04	238.00	72.77	318.00	80.56
80.00	56.21	160.00	65.23	240.00	72.97	320.00	80.75

Table D.3.2. Insertion Loss Values for Test Loop #2

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	16.52	82.00	56.91	162.00	60.93	242.00	68.19
4.00	19.15	84.00	57.40	164.00	61.03	244.00	68.46
6.00	21.81	86.00	57.85	166.00	61.13	246.00	68.74
8.00	24.22	88.00	58.28	168.00	61.24	248.00	69.02
10.00	26.38	90.00	58.66	170.00	61.35	250.00	69.30
12.00	28.32	92.00	59.00	172.00	61.47	252.00	69.59
14.00	30.09	94.00	59.29	174.00	61.58	254.00	69.88
16.00	31.70	96.00	59.53	176.00	61.71	256.00	70.17
18.00	33.18	98.00	59.72	178.00	61.84	258.00	70.47
20.00	34.55	100.00	59.87	180.00	61.97	260.00	70.78
22.00	35.81	102.00	60.00	182.00	62.10	262.00	71.09
24.00	36.98	104.00	60.09	184.00	62.24	264.00	71.40
26.00	38.08	106.00	60.15	186.00	62.38	266.00	71.72
28.00	39.10	108.00	60.18	188.00	62.52	268.00	72.04
30.00	40.06	110.00	60.20	190.00	62.67	270.00	72.36
32.00	40.96	112.00	60.19	192.00	62.82	272.00	72.69
34.00	41.82	114.00	60.18	194.00	62.98	274.00	73.01
36.00	42.63	116.00	60.16	196.00	63.14	276.00	73.34
38.00	43.40	118.00	60.14	198.00	63.30	278.00	73.66
40.00	44.14	120.00	60.11	200.00	63.46	280.00	73.98
42.00	44.85	122.00	60.09	202.00	63.65	282.00	74.30
44.00	45.53	124.00	60.08	204.00	63.85	284.00	74.62
46.00	46.19	126.00	60.06	206.00	64.04	286.00	74.92
48.00	46.83	128.00	60.06	208.00	64.24	288.00	75.22
50.00	47.46	130.00	60.06	210.00	64.44	290.00	75.51
52.00	48.10	132.00	60.06	212.00	64.65	292.00	75.79
54.00	48.74	134.00	60.08	214.00	64.86	294.00	76.05
56.00	49.36	136.00	60.10	216.00	65.07	296.00	76.30
58.00	49.98	138.00	60.12	218.00	65.29	298.00	76.54
60.00	50.59	140.00	60.16	220.00	65.51	300.00	76.76
62.00	51.20	142.00	60.20	222.00	65.73	302.00	76.96
64.00	51.80	144.00	60.25	224.00	65.96	304.00	77.15
66.00	52.40	146.00	60.30	226.00	66.19	306.00	77.32
68.00	52.99	148.00	60.36	228.00	66.42	308.00	77.47
70.00	53.58	150.00	60.43	230.00	66.66	310.00	77.60
72.00	54.17	152.00	60.50	232.00	66.91	312.00	77.73
74.00	54.74	154.00	60.57	234.00	67.15	314.00	77.83
76.00	55.31	156.00	60.65	236.00	67.41	316.00	77.93
78.00	55.86	158.00	60.74	238.00	67.66	318.00	78.01
80.00	56.40	160.00	60.83	240.00	67.92	320.00	78.09

Table D.3.3. Insertion Loss Values for Test Loop #3

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.96	82.00	48.89	162.00	67.00	242.00	69.16
4.00	17.38	84.00	49.19	164.00	66.93	244.00	69.40
6.00	19.90	86.00	49.49	166.00	66.82	246.00	69.64
8.00	22.22	88.00	49.81	168.00	66.68	248.00	69.88
10.00	24.31	90.00	50.14	170.00	66.52	250.00	70.13
12.00	26.20	92.00	50.48	172.00	66.33	252.00	70.38
14.00	27.92	94.00	50.83	174.00	66.12	254.00	70.64
16.00	29.50	96.00	51.20	176.00	65.91	256.00	70.91
18.00	30.96	98.00	51.58	178.00	65.69	258.00	71.18
20.00	32.31	100.00	51.98	180.00	65.47	260.00	71.46
22.00	33.57	102.00	52.42	182.00	65.27	262.00	71.75
24.00	34.75	104.00	52.87	184.00	65.07	264.00	72.04
26.00	35.86	106.00	53.34	186.00	64.90	266.00	72.33
28.00	36.90	108.00	53.82	188.00	64.75	268.00	72.63
30.00	37.89	110.00	54.32	190.00	64.63	270.00	72.93
32.00	38.81	112.00	54.83	192.00	64.55	272.00	73.24
34.00	39.68	114.00	55.36	194.00	64.49	274.00	73.54
36.00	40.49	116.00	55.91	196.00	64.47	276.00	73.84
38.00	41.26	118.00	56.48	198.00	64.48	278.00	74.13
40.00	41.96	120.00	57.07	200.00	64.53	280.00	74.42
42.00	42.61	122.00	57.68	202.00	64.62	282.00	74.71
44.00	43.20	124.00	58.31	204.00	64.74	284.00	74.99
46.00	43.73	126.00	58.95	206.00	64.89	286.00	75.26
48.00	44.20	128.00	59.61	208.00	65.07	288.00	75.52
50.00	44.62	130.00	60.29	210.00	65.26	290.00	75.77
52.00	45.01	132.00	60.98	212.00	65.48	292.00	76.01
54.00	45.36	134.00	61.67	214.00	65.71	294.00	76.24
56.00	45.67	136.00	62.35	216.00	65.96	296.00	76.45
58.00	45.95	138.00	63.02	218.00	66.21	298.00	76.65
60.00	46.20	140.00	63.67	220.00	66.47	300.00	76.84
62.00	46.45	142.00	64.29	222.00	66.73	302.00	77.01
64.00	46.68	144.00	64.86	224.00	66.99	304.00	77.16
66.00	46.91	146.00	65.37	226.00	67.25	306.00	77.30
68.00	47.13	148.00	65.82	228.00	67.51	308.00	77.43
70.00	47.36	150.00	66.20	230.00	67.75	310.00	77.54
72.00	47.60	152.00	66.51	232.00	68.00	312.00	77.64
74.00	47.84	154.00	66.74	234.00	68.24	314.00	77.73
76.00	48.09	156.00	66.89	236.00	68.47	316.00	77.80
78.00	48.34	158.00	66.99	238.00	68.70	318.00	77.87
80.00	48.61	160.00	67.02	240.00	68.93	320.00	77.93

Table D.3.4. Insertion Loss Values for Test Loop #4

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	16.01	82.00	46.75	162.00	55.00	242.00	62.29
4.00	18.70	84.00	46.99	164.00	55.18	244.00	62.48
6.00	21.29	86.00	47.23	166.00	55.36	246.00	62.66
8.00	23.52	88.00	47.46	168.00	55.54	248.00	62.85
10.00	25.45	90.00	47.69	170.00	55.73	250.00	63.03
12.00	27.14	92.00	47.91	172.00	55.91	252.00	63.21
14.00	28.63	94.00	48.13	174.00	56.09	254.00	63.39
16.00	29.98	96.00	48.34	176.00	56.27	256.00	63.56
18.00	31.19	98.00	48.55	178.00	56.45	258.00	63.74
20.00	32.29	100.00	48.76	180.00	56.63	260.00	63.91
22.00	33.29	102.00	48.99	182.00	56.80	262.00	64.09
24.00	34.21	104.00	49.21	184.00	56.98	264.00	64.26
26.00	35.06	106.00	49.43	186.00	57.16	266.00	64.44
28.00	35.84	108.00	49.66	188.00	57.34	268.00	64.61
30.00	36.56	110.00	49.87	190.00	57.51	270.00	64.79
32.00	37.23	112.00	50.09	192.00	57.69	272.00	64.96
34.00	37.86	114.00	50.30	194.00	57.86	274.00	65.14
36.00	38.45	116.00	50.51	196.00	58.04	276.00	65.31
38.00	39.00	118.00	50.72	198.00	58.21	278.00	65.49
40.00	39.52	120.00	50.93	200.00	58.39	280.00	65.66
42.00	40.01	122.00	51.13	202.00	58.58	282.00	65.84
44.00	40.47	124.00	51.34	204.00	58.76	284.00	66.01
46.00	40.91	126.00	51.54	206.00	58.95	286.00	66.19
48.00	41.32	128.00	51.74	208.00	59.14	288.00	66.36
50.00	41.71	130.00	51.94	210.00	59.33	290.00	66.54
52.00	42.12	132.00	52.14	212.00	59.51	292.00	66.71
54.00	42.50	134.00	52.34	214.00	59.70	294.00	66.89
56.00	42.87	136.00	52.54	216.00	59.88	296.00	67.06
58.00	43.23	138.00	52.73	218.00	60.07	298.00	67.23
60.00	43.58	140.00	52.93	220.00	60.26	300.00	67.41
62.00	43.91	142.00	53.12	222.00	60.44	302.00	67.58
64.00	44.24	144.00	53.31	224.00	60.63	304.00	67.76
66.00	44.55	146.00	53.50	226.00	60.81	306.00	67.93
68.00	44.85	148.00	53.69	228.00	61.00	308.00	68.10
70.00	45.15	150.00	53.88	230.00	61.18	310.00	68.28
72.00	45.43	152.00	54.07	232.00	61.37	312.00	68.45
74.00	45.71	154.00	54.26	234.00	61.55	314.00	68.63
76.00	45.98	156.00	54.44	236.00	61.74	316.00	68.80
78.00	46.24	158.00	54.63	238.00	61.92	318.00	68.97
80.00	46.50	160.00	54.81	240.00	62.11	320.00	69.15

Table D.3.5. Insertion Loss Values for Test Loop #5

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.78	82.00	47.82	162.00	52.38	242.00	59.19
4.00	16.74	84.00	48.13	164.00	52.48	244.00	59.43
6.00	18.89	86.00	48.43	166.00	52.59	246.00	59.67
8.00	20.91	88.00	48.70	168.00	52.70	248.00	59.92
10.00	22.74	90.00	48.94	170.00	52.81	250.00	60.17
12.00	24.39	92.00	49.17	172.00	52.93	252.00	60.41
14.00	25.89	94.00	49.37	174.00	53.05	254.00	60.66
16.00	27.25	96.00	49.55	176.00	53.17	256.00	60.91
18.00	28.50	98.00	49.71	178.00	53.30	258.00	61.16
20.00	29.66	100.00	49.85	180.00	53.42	260.00	61.41
22.00	30.73	102.00	50.00	182.00	53.55	262.00	61.67
24.00	31.72	104.00	50.13	184.00	53.69	264.00	61.92
26.00	32.64	106.00	50.25	186.00	53.82	266.00	62.17
28.00	33.51	108.00	50.35	188.00	53.96	268.00	62.43
30.00	34.33	110.00	50.45	190.00	54.11	270.00	62.68
32.00	35.10	112.00	50.53	192.00	54.25	272.00	62.93
34.00	35.83	114.00	50.61	194.00	54.40	274.00	63.18
36.00	36.52	116.00	50.68	196.00	54.55	276.00	63.42
38.00	37.18	118.00	50.75	198.00	54.70	278.00	63.66
40.00	37.82	120.00	50.82	200.00	54.86	280.00	63.90
42.00	38.43	122.00	50.88	202.00	55.03	282.00	64.13
44.00	39.01	124.00	50.94	204.00	55.21	284.00	64.35
46.00	39.58	126.00	51.00	206.00	55.39	286.00	64.57
48.00	40.12	128.00	51.06	208.00	55.57	288.00	64.78
50.00	40.65	130.00	51.12	210.00	55.76	290.00	64.99
52.00	41.19	132.00	51.18	212.00	55.95	292.00	65.18
54.00	41.72	134.00	51.24	214.00	56.14	294.00	65.37
56.00	42.23	136.00	51.31	216.00	56.34	296.00	65.55
58.00	42.73	138.00	51.37	218.00	56.54	298.00	65.72
60.00	43.23	140.00	51.44	220.00	56.74	300.00	65.88
62.00	43.71	142.00	51.51	222.00	56.95	302.00	66.03
64.00	44.18	144.00	51.58	224.00	57.15	304.00	66.17
66.00	44.64	146.00	51.66	226.00	57.37	306.00	66.31
68.00	45.08	148.00	51.74	228.00	57.58	308.00	66.43
70.00	45.52	150.00	51.82	230.00	57.80	310.00	66.55
72.00	45.94	152.00	51.90	232.00	58.02	312.00	66.66
74.00	46.35	154.00	51.99	234.00	58.25	314.00	66.77
76.00	46.75	156.00	52.08	236.00	58.48	316.00	66.87
78.00	47.12	158.00	52.18	238.00	58.71	318.00	66.96
80.00	47.48	160.00	52.28	240.00	58.95	320.00	67.05

Table D.3.6. Insertion Loss Values for Test Loop #6

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	15.14	82.00	44.72	162.00	55.91	242.00	73.04
4.00	17.67	84.00	44.96	164.00	56.27	244.00	73.50
6.00	20.14	86.00	45.20	166.00	56.64	246.00	73.97
8.00	22.29	88.00	45.44	168.00	57.02	248.00	74.43
10.00	24.14	90.00	45.67	170.00	57.40	250.00	74.90
12.00	25.76	92.00	45.90	172.00	57.78	252.00	75.35
14.00	27.20	94.00	46.13	174.00	58.17	254.00	75.80
16.00	28.49	96.00	46.36	176.00	58.56	256.00	76.26
18.00	29.65	98.00	46.58	178.00	58.96	258.00	76.71
20.00	30.71	100.00	46.81	180.00	59.36	260.00	77.16
22.00	31.68	102.00	47.06	182.00	59.76	262.00	77.61
24.00	32.57	104.00	47.32	184.00	60.17	264.00	78.06
26.00	33.39	106.00	47.58	186.00	60.58	266.00	78.50
28.00	34.15	108.00	47.83	188.00	60.99	268.00	78.95
30.00	34.85	110.00	48.09	190.00	61.41	270.00	79.39
32.00	35.50	112.00	48.35	192.00	61.83	272.00	79.82
34.00	36.11	114.00	48.61	194.00	62.25	274.00	80.25
36.00	36.68	116.00	48.87	196.00	62.67	276.00	80.67
38.00	37.21	118.00	49.13	198.00	63.10	278.00	81.08
40.00	37.71	120.00	49.40	200.00	63.53	280.00	81.49
42.00	38.18	122.00	49.67	202.00	63.96	282.00	81.88
44.00	38.63	124.00	49.94	204.00	64.41	284.00	82.26
46.00	39.05	126.00	50.21	206.00	64.85	286.00	82.63
48.00	39.45	128.00	50.49	208.00	65.29	288.00	82.98
50.00	39.82	130.00	50.77	210.00	65.74	290.00	83.32
52.00	40.21	132.00	51.05	212.00	66.19	292.00	83.64
54.00	40.59	134.00	51.34	214.00	66.64	294.00	83.93
56.00	40.95	136.00	51.63	216.00	67.09	296.00	84.21
58.00	41.30	138.00	51.93	218.00	67.54	298.00	84.46
60.00	41.63	140.00	52.23	220.00	67.99	300.00	84.69
62.00	41.95	142.00	52.54	222.00	68.45	302.00	84.89
64.00	42.27	144.00	52.85	224.00	68.90	304.00	85.07
66.00	42.57	146.00	53.17	226.00	69.36	306.00	85.23
68.00	42.86	148.00	53.49	228.00	69.81	308.00	85.36
70.00	43.15	150.00	53.82	230.00	70.27	310.00	85.46
72.00	43.42	152.00	54.16	232.00	70.73	312.00	85.55
74.00	43.69	154.00	54.49	234.00	71.19	314.00	85.61
76.00	43.96	156.00	54.84	236.00	71.65	316.00	85.66
78.00	44.22	158.00	55.19	238.00	72.11	318.00	85.69
80.00	44.47	160.00	55.54	240.00	72.58	320.00	85.70

Table D.3.7. Insertion Loss Values for Test Loop #7

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	15.08	82.00	43.34	162.00	50.23	242.00	56.05
4.00	16.89	84.00	43.56	164.00	50.37	244.00	56.20
6.00	18.90	86.00	43.77	166.00	50.52	246.00	56.35
8.00	20.80	88.00	43.98	168.00	50.66	248.00	56.50
10.00	22.51	90.00	44.18	170.00	50.80	250.00	56.65
12.00	24.05	92.00	44.38	172.00	50.94	252.00	56.80
14.00	25.44	94.00	44.57	174.00	51.08	254.00	56.95
16.00	26.71	96.00	44.76	176.00	51.22	256.00	57.10
18.00	27.88	98.00	44.94	178.00	51.36	258.00	57.24
20.00	28.96	100.00	45.12	180.00	51.50	260.00	57.39
22.00	29.95	102.00	45.31	182.00	51.64	262.00	57.54
24.00	30.88	104.00	45.51	184.00	51.77	264.00	57.69
26.00	31.73	106.00	45.70	186.00	51.91	266.00	57.83
28.00	32.52	108.00	45.89	188.00	52.05	268.00	57.98
30.00	33.27	110.00	46.07	190.00	52.19	270.00	58.13
32.00	33.96	112.00	46.25	192.00	52.32	272.00	58.28
34.00	34.61	114.00	46.43	194.00	52.46	274.00	58.42
36.00	35.21	116.00	46.61	196.00	52.59	276.00	58.57
38.00	35.78	118.00	46.79	198.00	52.73	278.00	58.72
40.00	36.32	120.00	46.96	200.00	52.86	280.00	58.87
42.00	36.82	122.00	47.13	202.00	53.02	282.00	59.01
44.00	37.30	124.00	47.30	204.00	53.17	284.00	59.16
46.00	37.74	126.00	47.46	206.00	53.32	286.00	59.31
48.00	38.17	128.00	47.63	208.00	53.48	288.00	59.45
50.00	38.57	130.00	47.79	210.00	53.63	290.00	59.60
52.00	38.97	132.00	47.95	212.00	53.78	292.00	59.75
54.00	39.35	134.00	48.11	214.00	53.94	294.00	59.89
56.00	39.72	136.00	48.27	216.00	54.09	296.00	60.04
58.00	40.07	138.00	48.43	218.00	54.24	298.00	60.19
60.00	40.40	140.00	48.59	220.00	54.39	300.00	60.33
62.00	40.72	142.00	48.74	222.00	54.54	302.00	60.48
64.00	41.03	144.00	48.89	224.00	54.70	304.00	60.63
66.00	41.33	146.00	49.05	226.00	54.85	306.00	60.77
68.00	41.61	148.00	49.20	228.00	55.00	308.00	60.92
70.00	41.88	150.00	49.35	230.00	55.15	310.00	61.06
72.00	42.15	152.00	49.50	232.00	55.30	312.00	61.21
74.00	42.40	154.00	49.64	234.00	55.45	314.00	61.36
76.00	42.65	156.00	49.79	236.00	55.60	316.00	61.50
78.00	42.89	158.00	49.94	238.00	55.75	318.00	61.65
80.00	43.12	160.00	50.08	240.00	55.90	320.00	61.79

Table D.3.8. Insertion Loss Values for Test Loop #8

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.50	82.00	43.92	162.00	56.86	242.00	57.68
4.00	16.61	84.00	44.27	164.00	56.83	244.00	57.80
6.00	18.81	86.00	44.62	166.00	56.78	246.00	57.91
8.00	20.79	88.00	44.97	168.00	56.73	248.00	58.03
10.00	22.52	90.00	45.33	170.00	56.67	250.00	58.16
12.00	24.05	92.00	45.69	172.00	56.61	252.00	58.27
14.00	25.42	94.00	46.05	174.00	56.55	254.00	58.38
16.00	26.64	96.00	46.42	176.00	56.49	256.00	58.50
18.00	27.76	98.00	46.79	178.00	56.43	258.00	58.62
20.00	28.78	100.00	47.17	180.00	56.38	260.00	58.74
22.00	29.73	102.00	47.58	182.00	56.33	262.00	58.87
24.00	30.60	104.00	48.00	184.00	56.29	264.00	58.99
26.00	31.41	106.00	48.42	186.00	56.26	266.00	59.12
28.00	32.16	108.00	48.85	188.00	56.22	268.00	59.25
30.00	32.86	110.00	49.28	190.00	56.20	270.00	59.38
32.00	33.52	112.00	49.72	192.00	56.18	272.00	59.52
34.00	34.14	114.00	50.16	194.00	56.17	274.00	59.65
36.00	34.71	116.00	50.61	196.00	56.17	276.00	59.79
38.00	35.26	118.00	51.05	198.00	56.17	278.00	59.93
40.00	35.77	120.00	51.50	200.00	56.17	280.00	60.07
42.00	36.26	122.00	51.95	202.00	56.20	282.00	60.22
44.00	36.73	124.00	52.40	204.00	56.23	284.00	60.36
46.00	37.17	126.00	52.84	206.00	56.26	286.00	60.51
48.00	37.59	128.00	53.27	208.00	56.30	288.00	60.66
50.00	38.00	130.00	53.70	210.00	56.34	290.00	60.81
52.00	38.43	132.00	54.11	212.00	56.39	292.00	60.96
54.00	38.84	134.00	54.50	214.00	56.45	294.00	61.11
56.00	39.24	136.00	54.87	216.00	56.51	296.00	61.27
58.00	39.63	138.00	55.22	218.00	56.58	298.00	61.43
60.00	40.01	140.00	55.54	220.00	56.65	300.00	61.59
62.00	40.39	142.00	55.83	222.00	56.72	302.00	61.75
64.00	40.76	144.00	56.09	224.00	56.80	304.00	61.91
66.00	41.12	146.00	56.30	226.00	56.88	306.00	62.07
68.00	41.48	148.00	56.48	228.00	56.97	308.00	62.24
70.00	41.83	150.00	56.63	230.00	57.06	310.00	62.40
72.00	42.18	152.00	56.74	232.00	57.16	312.00	62.57
74.00	42.53	154.00	56.81	234.00	57.25	314.00	62.74
76.00	42.88	156.00	56.86	236.00	57.36	316.00	62.91
78.00	43.23	158.00	56.88	238.00	57.46	318.00	63.08
80.00	43.57	160.00	56.88	240.00	57.57	320.00	63.26

Table D.3.9. Insertion Loss Values for Test Loop #9

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	13.21	82.00	51.46	162.00	47.02	242.00	52.93
4.00	14.77	84.00	51.88	164.00	46.99	244.00	53.27
6.00	16.63	86.00	52.25	166.00	46.96	246.00	53.61
8.00	18.47	88.00	52.56	168.00	46.95	248.00	53.97
10.00	20.19	90.00	52.80	170.00	46.95	250.00	54.33
12.00	21.80	92.00	52.99	172.00	46.96	252.00	54.71
14.00	23.28	94.00	53.11	174.00	46.98	254.00	55.09
16.00	24.66	96.00	53.17	176.00	47.01	256.00	55.48
18.00	25.96	98.00	53.17	178.00	47.04	258.00	55.87
20.00	27.17	100.00	53.12	180.00	47.09	260.00	56.27
22.00	28.31	102.00	53.03	182.00	47.14	262.00	56.68
24.00	29.38	104.00	52.89	184.00	47.20	264.00	57.09
26.00	30.40	106.00	52.71	186.00	47.27	266.00	57.50
28.00	31.36	108.00	52.50	188.00	47.35	268.00	57.91
30.00	32.29	110.00	52.26	190.00	47.43	270.00	58.32
32.00	33.17	112.00	51.99	192.00	47.52	272.00	58.72
34.00	34.03	114.00	51.71	194.00	47.62	274.00	59.11
36.00	34.86	116.00	51.41	196.00	47.73	276.00	59.50
38.00	35.67	118.00	51.10	198.00	47.85	278.00	59.88
40.00	36.46	120.00	50.80	200.00	47.98	280.00	60.24
42.00	37.24	122.00	50.49	202.00	48.13	282.00	60.58
44.00	38.02	124.00	50.18	204.00	48.29	284.00	60.91
46.00	38.78	126.00	49.89	206.00	48.45	286.00	61.21
48.00	39.54	128.00	49.60	208.00	48.63	288.00	61.49
50.00	40.30	130.00	49.33	210.00	48.81	290.00	61.75
52.00	41.08	132.00	49.07	212.00	49.01	292.00	61.98
54.00	41.86	134.00	48.83	214.00	49.21	294.00	62.18
56.00	42.64	136.00	48.60	216.00	49.42	296.00	62.35
58.00	43.41	138.00	48.38	218.00	49.63	298.00	62.50
60.00	44.19	140.00	48.19	220.00	49.86	300.00	62.61
62.00	44.96	142.00	48.01	222.00	50.09	302.00	62.70
64.00	45.72	144.00	47.84	224.00	50.34	304.00	62.75
66.00	46.47	146.00	47.70	226.00	50.59	306.00	62.78
68.00	47.20	148.00	47.56	228.00	50.85	308.00	62.79
70.00	47.91	150.00	47.45	230.00	51.12	310.00	62.77
72.00	48.60	152.00	47.34	232.00	51.40	312.00	62.72
74.00	49.25	154.00	47.25	234.00	51.69	314.00	62.66
76.00	49.87	156.00	47.17	236.00	51.98	316.00	62.58
78.00	50.45	158.00	47.11	238.00	52.29	318.00	62.48
80.00	50.98	160.00	47.06	240.00	52.61	320.00	62.37

Table D.3.10. Insertion Loss Values for Test Loop #10

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.20	82.00	42.00	162.00	57.37	242.00	56.63
4.00	16.30	84.00	42.35	164.00	57.25	244.00	56.73
6.00	18.46	86.00	42.71	166.00	57.12	246.00	56.85
8.00	20.38	88.00	43.06	168.00	56.97	248.00	56.96
10.00	22.05	90.00	43.43	170.00	56.82	250.00	57.08
12.00	23.51	92.00	43.79	172.00	56.67	252.00	57.19
14.00	24.80	94.00	44.17	174.00	56.52	254.00	57.29
16.00	25.95	96.00	44.55	176.00	56.38	256.00	57.41
18.00	26.99	98.00	44.94	178.00	56.24	258.00	57.52
20.00	27.94	100.00	45.34	180.00	56.12	260.00	57.64
22.00	28.82	102.00	45.77	182.00	56.01	262.00	57.76
24.00	29.63	104.00	46.21	184.00	55.90	264.00	57.88
26.00	30.37	106.00	46.67	186.00	55.81	266.00	58.00
28.00	31.07	108.00	47.13	188.00	55.73	268.00	58.13
30.00	31.71	110.00	47.61	190.00	55.66	270.00	58.25
32.00	32.31	112.00	48.09	192.00	55.60	272.00	58.38
34.00	32.87	114.00	48.59	194.00	55.55	274.00	58.51
36.00	33.40	116.00	49.10	196.00	55.51	276.00	58.65
38.00	33.89	118.00	49.62	198.00	55.48	278.00	58.78
40.00	34.36	120.00	50.15	200.00	55.46	280.00	58.92
42.00	34.81	122.00	50.69	202.00	55.45	282.00	59.06
44.00	35.23	124.00	51.24	204.00	55.44	284.00	59.20
46.00	35.63	126.00	51.80	206.00	55.45	286.00	59.34
48.00	36.02	128.00	52.36	208.00	55.46	288.00	59.48
50.00	36.39	130.00	52.93	210.00	55.49	290.00	59.63
52.00	36.78	132.00	53.49	212.00	55.51	292.00	59.78
54.00	37.16	134.00	54.05	214.00	55.55	294.00	59.93
56.00	37.53	136.00	54.59	216.00	55.59	296.00	60.08
58.00	37.89	138.00	55.11	218.00	55.64	298.00	60.23
60.00	38.24	140.00	55.60	220.00	55.70	300.00	60.38
62.00	38.59	142.00	56.05	222.00	55.76	302.00	60.53
64.00	38.93	144.00	56.45	224.00	55.82	304.00	60.69
66.00	39.27	146.00	56.80	226.00	55.89	306.00	60.85
68.00	39.61	148.00	57.08	228.00	55.97	308.00	61.01
70.00	39.95	150.00	57.30	230.00	56.05	310.00	61.17
72.00	40.29	152.00	57.45	232.00	56.14	312.00	61.33
74.00	40.63	154.00	57.53	234.00	56.23	314.00	61.49
76.00	40.97	156.00	57.56	236.00	56.32	316.00	61.66
78.00	41.31	158.00	57.54	238.00	56.42	318.00	61.82
80.00	41.65	160.00	57.47	240.00	56.52	320.00	61.99

Table D.3.11. Insertion Loss Values for Test Loop #11

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.05	82.00	44.33	162.00	47.58	242.00	53.12
4.00	15.47	84.00	44.62	164.00	47.65	244.00	53.33
6.00	17.17	86.00	44.89	166.00	47.72	246.00	53.55
8.00	18.87	88.00	45.13	168.00	47.80	248.00	53.76
10.00	20.45	90.00	45.35	170.00	47.88	250.00	53.98
12.00	21.91	92.00	45.55	172.00	47.96	252.00	54.20
14.00	23.24	94.00	45.73	174.00	48.05	254.00	54.42
16.00	24.48	96.00	45.88	176.00	48.14	256.00	54.65
18.00	25.64	98.00	46.01	178.00	48.23	258.00	54.87
20.00	26.71	100.00	46.13	180.00	48.32	260.00	55.10
22.00	27.72	102.00	46.24	182.00	48.42	262.00	55.33
24.00	28.66	104.00	46.34	184.00	48.52	264.00	55.56
26.00	29.54	106.00	46.42	186.00	48.62	266.00	55.78
28.00	30.38	108.00	46.49	188.00	48.73	268.00	56.01
30.00	31.18	110.00	46.55	190.00	48.84	270.00	56.24
32.00	31.93	112.00	46.60	192.00	48.95	272.00	56.46
34.00	32.65	114.00	46.64	194.00	49.07	274.00	56.68
36.00	33.34	116.00	46.67	196.00	49.18	276.00	56.90
38.00	33.99	118.00	46.71	198.00	49.30	278.00	57.11
40.00	34.62	120.00	46.73	200.00	49.43	280.00	57.32
42.00	35.23	122.00	46.76	202.00	49.57	282.00	57.53
44.00	35.81	124.00	46.78	204.00	49.72	284.00	57.73
46.00	36.38	126.00	46.81	206.00	49.87	286.00	57.92
48.00	36.92	128.00	46.83	208.00	50.03	288.00	58.10
50.00	37.45	130.00	46.85	210.00	50.18	290.00	58.28
52.00	37.99	132.00	46.88	212.00	50.34	292.00	58.45
54.00	38.50	134.00	46.91	214.00	50.50	294.00	58.61
56.00	39.01	136.00	46.94	216.00	50.67	296.00	58.76
58.00	39.50	138.00	46.97	218.00	50.84	298.00	58.90
60.00	39.98	140.00	47.00	220.00	51.01	300.00	59.03
62.00	40.45	142.00	47.04	222.00	51.19	302.00	59.16
64.00	40.91	144.00	47.08	224.00	51.37	304.00	59.27
66.00	41.35	146.00	47.12	226.00	51.55	306.00	59.38
68.00	41.78	148.00	47.17	228.00	51.73	308.00	59.48
70.00	42.19	150.00	47.22	230.00	51.92	310.00	59.57
72.00	42.59	152.00	47.27	232.00	52.11	312.00	59.65
74.00	42.98	154.00	47.32	234.00	52.31	314.00	59.73
76.00	43.35	156.00	47.38	236.00	52.51	316.00	59.81
78.00	43.70	158.00	47.44	238.00	52.71	318.00	59.87
80.00	44.03	160.00	47.51	240.00	52.91	320.00	59.94

Table D.3.12. Insertion Loss Values for Test Loop #12

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.05	82.00	38.78	162.00	45.45	242.00	51.29
4.00	15.65	84.00	38.98	164.00	45.59	244.00	51.44
6.00	17.47	86.00	39.17	166.00	45.74	246.00	51.59
8.00	19.21	88.00	39.35	168.00	45.88	248.00	51.73
10.00	20.78	90.00	39.53	170.00	46.03	250.00	51.88
12.00	22.19	92.00	39.71	172.00	46.17	252.00	52.03
14.00	23.45	94.00	39.89	174.00	46.32	254.00	52.17
16.00	24.59	96.00	40.06	176.00	46.46	256.00	52.31
18.00	25.63	98.00	40.23	178.00	46.60	258.00	52.45
20.00	26.58	100.00	40.39	180.00	46.74	260.00	52.60
22.00	27.44	102.00	40.58	182.00	46.88	262.00	52.74
24.00	28.24	104.00	40.77	184.00	47.02	264.00	52.88
26.00	28.97	106.00	40.95	186.00	47.16	266.00	53.02
28.00	29.65	108.00	41.13	188.00	47.30	268.00	53.17
30.00	30.27	110.00	41.31	190.00	47.44	270.00	53.31
32.00	30.85	112.00	41.49	192.00	47.58	272.00	53.45
34.00	31.38	114.00	41.66	194.00	47.72	274.00	53.59
36.00	31.88	116.00	41.84	196.00	47.86	276.00	53.74
38.00	32.35	118.00	42.01	198.00	48.00	278.00	53.88
40.00	32.79	120.00	42.18	200.00	48.14	280.00	54.02
42.00	33.20	122.00	42.35	202.00	48.29	282.00	54.16
44.00	33.59	124.00	42.51	204.00	48.44	284.00	54.30
46.00	33.96	126.00	42.68	206.00	48.59	286.00	54.45
48.00	34.31	128.00	42.84	208.00	48.74	288.00	54.59
50.00	34.64	130.00	43.00	210.00	48.89	290.00	54.73
52.00	34.98	132.00	43.16	212.00	49.05	292.00	54.87
54.00	35.30	134.00	43.32	214.00	49.20	294.00	55.01
56.00	35.62	136.00	43.48	216.00	49.35	296.00	55.16
58.00	35.92	138.00	43.64	218.00	49.50	298.00	55.30
60.00	36.20	140.00	43.79	220.00	49.65	300.00	55.44
62.00	36.48	142.00	43.95	222.00	49.80	302.00	55.58
64.00	36.75	144.00	44.10	224.00	49.95	304.00	55.72
66.00	37.00	146.00	44.25	226.00	50.10	306.00	55.86
68.00	37.25	148.00	44.41	228.00	50.25	308.00	56.01
70.00	37.49	150.00	44.56	230.00	50.40	310.00	56.15
72.00	37.72	152.00	44.71	232.00	50.54	312.00	56.29
74.00	37.95	154.00	44.86	234.00	50.69	314.00	56.43
76.00	38.17	156.00	45.01	236.00	50.84	316.00	56.57
78.00	38.38	158.00	45.15	238.00	50.99	318.00	56.72
80.00	38.58	160.00	45.30	240.00	51.14	320.00	56.86

Table D.3.13. Insertion Loss Values for Test Loop #13

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	13.38	82.00	45.43	162.00	46.96	242.00	52.77
4.00	14.78	84.00	45.85	164.00	46.97	244.00	53.07
6.00	16.49	86.00	46.24	166.00	46.99	246.00	53.37
8.00	18.21	88.00	46.60	168.00	47.01	248.00	53.67
10.00	19.84	90.00	46.92	170.00	47.04	250.00	53.99
12.00	21.35	92.00	47.22	172.00	47.08	252.00	54.30
14.00	22.75	94.00	47.47	174.00	47.13	254.00	54.62
16.00	24.04	96.00	47.69	176.00	47.18	256.00	54.95
18.00	25.24	98.00	47.87	178.00	47.24	258.00	55.28
20.00	26.35	100.00	48.02	180.00	47.30	260.00	55.62
22.00	27.38	102.00	48.15	182.00	47.37	262.00	55.95
24.00	28.35	104.00	48.25	184.00	47.45	264.00	56.29
26.00	29.25	106.00	48.31	186.00	47.54	266.00	56.63
28.00	30.10	108.00	48.35	188.00	47.63	268.00	56.96
30.00	30.90	110.00	48.37	190.00	47.72	270.00	57.30
32.00	31.66	112.00	48.36	192.00	47.83	272.00	57.63
34.00	32.38	114.00	48.33	194.00	47.93	274.00	57.95
36.00	33.06	116.00	48.29	196.00	48.05	276.00	58.27
38.00	33.72	118.00	48.24	198.00	48.17	278.00	58.58
40.00	34.35	120.00	48.17	200.00	48.30	280.00	58.87
42.00	34.96	122.00	48.10	202.00	48.44	282.00	59.16
44.00	35.55	124.00	48.02	204.00	48.60	284.00	59.43
46.00	36.12	126.00	47.93	206.00	48.76	286.00	59.68
48.00	36.68	128.00	47.85	208.00	48.92	288.00	59.92
50.00	37.22	130.00	47.76	210.00	49.09	290.00	60.15
52.00	37.78	132.00	47.67	212.00	49.27	292.00	60.35
54.00	38.33	134.00	47.59	214.00	49.46	294.00	60.53
56.00	38.87	136.00	47.50	216.00	49.65	296.00	60.70
58.00	39.41	138.00	47.43	218.00	49.84	298.00	60.84
60.00	39.94	140.00	47.35	220.00	50.05	300.00	60.97
62.00	40.47	142.00	47.28	222.00	50.26	302.00	61.07
64.00	41.00	144.00	47.22	224.00	50.48	304.00	61.15
66.00	41.52	146.00	47.16	226.00	50.70	306.00	61.22
68.00	42.04	148.00	47.11	228.00	50.94	308.00	61.27
70.00	42.55	150.00	47.07	230.00	51.18	310.00	61.30
72.00	43.06	152.00	47.03	232.00	51.42	312.00	61.32
74.00	43.56	154.00	47.00	234.00	51.68	314.00	61.32
76.00	44.06	156.00	46.98	236.00	51.94	316.00	61.32
78.00	44.53	158.00	46.97	238.00	52.21	318.00	61.30
80.00	44.99	160.00	46.96	240.00	52.49	320.00	61.27

Table D.3.14. Insertion Loss Values for Test Loop #14

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	12.71	82.00	39.58	162.00	49.92	242.00	50.54
4.00	14.58	84.00	39.82	164.00	49.79	244.00	50.74
6.00	16.63	86.00	40.07	166.00	49.65	246.00	50.95
8.00	18.54	88.00	40.32	168.00	49.51	248.00	51.16
10.00	20.26	90.00	40.59	170.00	49.38	250.00	51.37
12.00	21.81	92.00	40.86	172.00	49.25	252.00	51.58
14.00	23.21	94.00	41.15	174.00	49.12	254.00	51.80
16.00	24.47	96.00	41.45	176.00	49.01	256.00	52.02
18.00	25.63	98.00	41.76	178.00	48.90	258.00	52.24
20.00	26.69	100.00	42.08	180.00	48.80	260.00	52.47
22.00	27.68	102.00	42.44	182.00	48.71	262.00	52.70
24.00	28.59	104.00	42.81	184.00	48.64	264.00	52.94
26.00	29.43	106.00	43.19	186.00	48.57	266.00	53.18
28.00	30.22	108.00	43.58	188.00	48.51	268.00	53.42
30.00	30.95	110.00	43.99	190.00	48.46	270.00	53.67
32.00	31.64	112.00	44.41	192.00	48.42	272.00	53.91
34.00	32.29	114.00	44.83	194.00	48.39	274.00	54.16
36.00	32.90	116.00	45.26	196.00	48.37	276.00	54.40
38.00	33.47	118.00	45.69	198.00	48.36	278.00	54.65
40.00	34.00	120.00	46.13	200.00	48.36	280.00	54.89
42.00	34.49	122.00	46.57	202.00	48.37	282.00	55.13
44.00	34.94	124.00	47.00	204.00	48.39	284.00	55.37
46.00	35.35	126.00	47.43	206.00	48.42	286.00	55.60
48.00	35.72	128.00	47.84	208.00	48.46	288.00	55.82
50.00	36.04	130.00	48.24	210.00	48.51	290.00	56.04
52.00	36.35	132.00	48.61	212.00	48.57	292.00	56.24
54.00	36.63	134.00	48.96	214.00	48.63	294.00	56.44
56.00	36.87	136.00	49.28	216.00	48.71	296.00	56.63
58.00	37.10	138.00	49.56	218.00	48.80	298.00	56.80
60.00	37.31	140.00	49.81	220.00	48.90	300.00	56.96
62.00	37.51	142.00	50.01	222.00	49.00	302.00	57.11
64.00	37.70	144.00	50.17	224.00	49.12	304.00	57.24
66.00	37.90	146.00	50.28	226.00	49.24	306.00	57.36
68.00	38.09	148.00	50.35	228.00	49.37	308.00	57.47
70.00	38.28	150.00	50.38	230.00	49.52	310.00	57.57
72.00	38.48	152.00	50.37	232.00	49.67	312.00	57.65
74.00	38.69	154.00	50.33	234.00	49.83	314.00	57.73
76.00	38.90	156.00	50.25	236.00	49.99	316.00	57.79
78.00	39.12	158.00	50.16	238.00	50.17	318.00	57.85
80.00	39.35	160.00	50.05	240.00	50.35	320.00	57.90

Table D.3.15. Insertion Loss Values for Test Loop #15

Freq	Loss	Freq	Loss	Freq	Loss	Freq	Loss
2.00	14.01	82.00	38.50	162.00	44.64	242.00	49.83
4.00	15.35	84.00	38.69	164.00	44.77	244.00	49.96
6.00	16.95	86.00	38.88	166.00	44.90	246.00	50.09
8.00	18.54	88.00	39.07	168.00	45.02	248.00	50.23
10.00	20.02	90.00	39.24	170.00	45.15	250.00	50.36
12.00	21.37	92.00	39.42	172.00	45.28	252.00	50.49
14.00	22.59	94.00	39.59	174.00	45.40	254.00	50.62
16.00	23.71	96.00	39.76	176.00	45.53	256.00	50.76
18.00	24.74	98.00	39.92	178.00	45.65	258.00	50.89
20.00	25.69	100.00	40.08	180.00	45.77	260.00	51.02
22.00	26.57	102.00	40.26	182.00	45.90	262.00	51.15
24.00	27.38	104.00	40.43	184.00	46.02	264.00	51.28
26.00	28.14	106.00	40.60	186.00	46.14	266.00	51.41
28.00	28.84	108.00	40.77	188.00	46.26	268.00	51.54
30.00	29.50	110.00	40.93	190.00	46.39	270.00	51.68
32.00	30.12	112.00	41.10	192.00	46.51	272.00	51.81
34.00	30.69	114.00	41.26	194.00	46.63	274.00	51.94
36.00	31.23	116.00	41.41	196.00	46.75	276.00	52.07
38.00	31.74	118.00	41.57	198.00	46.87	278.00	52.20
40.00	32.22	120.00	41.73	200.00	46.99	280.00	52.33
42.00	32.67	122.00	41.88	202.00	47.12	282.00	52.46
44.00	33.09	124.00	42.03	204.00	47.26	284.00	52.59
46.00	33.49	126.00	42.18	206.00	47.40	286.00	52.72
48.00	33.87	128.00	42.32	208.00	47.54	288.00	52.85
50.00	34.23	130.00	42.47	210.00	47.67	290.00	52.98
52.00	34.59	132.00	42.61	212.00	47.81	292.00	53.11
54.00	34.93	134.00	42.76	214.00	47.94	294.00	53.24
56.00	35.25	136.00	42.90	216.00	48.08	296.00	53.37
58.00	35.57	138.00	43.04	218.00	48.22	298.00	53.50
60.00	35.86	140.00	43.18	220.00	48.35	300.00	53.64
62.00	36.15	142.00	43.32	222.00	48.49	302.00	53.77
64.00	36.43	144.00	43.45	224.00	48.62	304.00	53.90
66.00	36.69	146.00	43.59	226.00	48.76	306.00	54.03
68.00	36.94	148.00	43.72	228.00	48.89	308.00	54.16
70.00	37.19	150.00	43.86	230.00	49.02	310.00	54.29
72.00	37.43	152.00	43.99	232.00	49.16	312.00	54.42
74.00	37.65	154.00	44.12	234.00	49.29	314.00	54.55
76.00	37.87	156.00	44.25	236.00	49.43	316.00	54.68
78.00	38.09	158.00	44.38	238.00	49.56	318.00	54.81
80.00	38.30	160.00	44.51	240.00	49.69	320.00	54.93

NIST-114A
(REV. 3-90)

U.S. DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

BIBLIOGRAPHIC DATA SHEET

1. PUBLICATION OR REPORT NUMBER
NIST/SP-823/2

2. PERFORMING ORGANIZATION REPORT NUMBER

3. PUBLICATION DATE
March 1992

4. TITLE AND SUBTITLE

Integrated Services Digital Network Conformance Testing
Layer 1 - Physical Layer, Part 2 - Basic Rate U Interface, User Side

5. AUTHOR(S)

Daniel P. Stokesberry and Kathleen M. Roberts, Editors

6. PERFORMING ORGANIZATION (IF JOINT OR OTHER THAN NIST, SEE INSTRUCTIONS)

U.S. DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
GAITHERSBURG, MD 20899

7. CONTRACT/GRANT NUMBER

8. TYPE OF REPORT AND PERIOD COVERED
Final

9. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS (STREET, CITY, STATE, ZIP)

Same as item #6

10. SUPPLEMENTARY NOTES

11. ABSTRACT (A 200-WORD OR LESS FACTUAL SUMMARY OF MOST SIGNIFICANT INFORMATION. IF DOCUMENT INCLUDES A SIGNIFICANT BIBLIOGRAPHY OR LITERATURE SURVEY, MENTION IT HERE.)

The American National Standard for Telecommunications (ANS) T1.601-1988 specifies the minimal set of requirements to provide for satisfactory transmission between the network and the Network Termination (NT). It describes both the physical interface and the electrical characteristics of the signals appearing at the network side of the NT, commonly called the U interface point, or U reference point. Equipment designed to operate on the North American Integrated Services Digital Network (ISDN) Basic Access U Interface must conform with this set of minimal requirements.

This document describes a set of conformance test specifications for all NTs connected to the Basic Rate ISDN user-network interface. These tests were developed and approved by members of the North American ISDN Users' Forum.

12. KEY WORDS (6 TO 12 ENTRIES; ALPHABETICAL ORDER; CAPITALIZE ONLY PROPER NAMES; AND SEPARATE KEY WORDS BY SEMICOLONS)

Abstract Test Suites; Basic Rate Interface, BRI; Conformance Testing; Digital Subscriber Line; ISDN; Network Termination, NT; Physical Layer; Static Conformance Requirements; U Interface; U Reference Point

13. AVAILABILITY

X	UNLIMITED
	FOR OFFICIAL DISTRIBUTION. DO NOT RELEASE TO NATIONAL TECHNICAL INFORMATION SERVICE (NTIS).
X	ORDER FROM SUPERINTENDENT OF DOCUMENTS, U.S. GOVERNMENT PRINTING OFFICE, WASHINGTON, DC 20402.
X	ORDER FROM NATIONAL TECHNICAL INFORMATION SERVICE (NTIS), SPRINGFIELD, VA 22161.

14. NUMBER OF PRINTED PAGES
96

15. PRICE

ELECTRONIC FORM

* U.S. G.P.O.:1992-311-891:60453

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